

Publications

Hardware/Software Co-Design

Prof. Dr.-Ing. Jürgen Teich

2026

- [Heidorn C.](#), Hannig F., Riedelbauch D., Strohmeyer C., Teich J.:
[Entropy Sampling-Based Neural Architecture Search for Resource-Constrained Microcontroller Targets](#)
Conference on Design, Automation and Test in Europe (DATE) (Verona, 20. April 2026 - 22. April 2026)
BibTeX: [Download](#)
- [Heidorn C.](#), Hannig F., Riedelbauch D., Strohmeyer C., Teich J.:
[OpTC - Automatic Compression and Performance Estimation for Deployment of Neural Networks on AURIX TC3xx Microcontrollers](#)
In: **Communications in Computer and Information Science** (2026)
ISSN: 1865-0929
BibTeX: [Download](#)
- Sotiropoulos G., Frombach F., Höfer J., Harbaum T., Becker J., Thorøe Hl., Meyers V., Tahoori M., Demirdag Z., Sikal MB., Nassar H., Khdr H., Henkel J., Wolters C., van Kempen P., Geier J., Schlichtmann U., Sesli B., Sabih M., Wittmann J., Hannig F., Teich J., Steiner L., Wehn N., Shelkamy Ali M., Schmitz P., Kunz W., Kögler S., Sigl G.:
[Multi-Partner Project: A Holistic and Open-Source Approach to Efficient, Secure and Reliable AI Hardware Deployment in DI-EDA](#)
Design, Automation and Test in Europe Conference (Verona, 20. April 2026 - 22. April 2026)
In: **Proceedings of the Conference on Design, Automation and Test in Europe (DATE) 2026**
BibTeX: [Download](#)

2025

- Darne B., Karim A., Matrangolo PA., [Falk J.](#), O'Connor I., Marchand C., Bosio A., Teich J.:
[FeMFET-based High Performance, Ultra-Low Power Memory Cells for Reliable State Retention of Dataflow Networks](#)
38th IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems; Special Session (Barcelona, Spain, 21. Oktober 2025 - 23. Oktober 2025)
In: **Proceedings of the 38th IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems 2025**
BibTeX: [Download](#)
- Deutel M., Kontes G., Mutschler C., Teich J.:
[Combining Multi-Objective Bayesian Optimization with Reinforcement Learning for TinyML](#)
In: **ACM Transactions on Evolutionary Learning and Optimization 5 (2025)**, p. 1-21
ISSN: 2688-299X
DOI: [10.1145/3715012](#)
BibTeX: [Download](#)
- Deutel M., Kontes G., Mutschler C., Teich J.:
[Multi-Objective Bayesian Optimization with Reinforcement Learning for Edge Deployment of DNNs on Microcontrollers](#)
The Genetic and Evolutionary Computation Conference (GECCO) (Málaga, 14. Juli 2025 - 18. Juli 2025)
In: ACM (ed.): **GECCO '25 Companion: Proceedings of the Genetic and Evolutionary Computation Conference Companion 2025**
DOI: [10.1145/3712255.3734232](#)
BibTeX: [Download](#)
- Deutel M., Mutschler C., Teich J.:
[microYOLO: Towards Single-Shot Object Detection on Microcontrollers](#)
4th Workshop on IoT, Edge, and Mobile for Embedded Machine Learning (ITEM) (Torino, 18. September 2023 - 22. September 2023)
In: University of Turin (ed.): **International Workshops of ECML PKDD 2023**,

Turin, Italy, September 18–22, 2023, Revised Selected Papers, Part V 2025

DOI: [10.1007/978-3-031-74643-7_13](https://doi.org/10.1007/978-3-031-74643-7_13)

BibTeX: [Download](#)

- Deutel M., Plinge A., Seuss D., Mutschler C., Hannig F., Teich J.:
[**Unsupervised Learning of Variational Autoencoders on Cortex-M Microcontrollers**](#)
IEEE 18th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoc) (Singapore, 15. Dezember 2025 - 18. Dezember 2025)
In: **Proceedings of the IEEE 18th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoc) 2025**
DOI: [10.1109/MCSoc67473.2025.00079](https://doi.org/10.1109/MCSoc67473.2025.00079)
BibTeX: [Download](#)
- Esper K., Wildermann S., Teich J.:
[**Response Range Optimization for Run-Time Requirement Enforcement on MPSocs**](#)
30th Asia and South Pacific Design Automation Conference ASP-DAC 2025 (Tokyo, 20. Januar 2025 - 23. Januar 2025)
In: **Proceedings of the 30th Asia and South Pacific Design Automation Conference 2025**
DOI: [10.1145/3658617.3697552](https://doi.org/10.1145/3658617.3697552)
BibTeX: [Download](#)
- Esper K., Wildermann S., Teich J.:
[**Run-time Requirement Enforcement of Safety Requirements of Human-Robot Interactions**](#)
International Conference on Automation, Robotics, and Applications (Zagreb, 12. Februar 2025 - 14. Februar 2025)
In: **2025 11th International Conference on Automation, Robotics, and Applications (ICARA) 2025**
DOI: [10.1109/ICARA64554.2025.10977632](https://doi.org/10.1109/ICARA64554.2025.10977632)
URL: <https://ieeexplore.ieee.org/document/10977632>
BibTeX: [Download](#)
- Groth S., [Heidorn C.](#), Schmid M., Teich J., Hannig F.:
[**Latency-Constrained Neural Architecture Search for U-Nets on Graphics**](#)

Processing Units

28th Workshop on Methods and Description Languages for Modelling and Verification of Circuits and Systems (MBMV) (Rostock, 11. März 2025 - 12. März 2025)

In: **Proceedings of the 28th Workshop on Methods and Description Languages for Modelling and Verification of Circuits and Systems (MBMV)**, 2025

URL: <https://ieeexplore.ieee.org/document/11047216>

BibTeX: [Download](#)

- Hahn T., Hofmann J., Wildermann S., Teich J.:

FSST Compression of JSON Data on FPGAs

38th GI/ITG International Conference on Architecture of Computing Systems (Kiel, 22. April 2025 - 24. April 2025)

BibTeX: [Download](#)

- Hahn T., Langohr M., Becher A., Beena Gopalakrishnan Nair L., Meyer-Wegener K., Teich J., Wildermann S.:

ReProVide: Query Optimization and Near-Data Processing on Reconfigurable SoCs for Big Data Analysis

In: **Scalable Data Management for Future Hardware**, 2025, p. 171-197

ISBN: 9783031740961

DOI: [10.1007/978-3-031-74097-8_7](https://doi.org/10.1007/978-3-031-74097-8_7)

BibTeX: [Download](#)

- Hahn T., Langohr M., Meißner S., Döring B., Wildermann S., Meyer-Wegener K., Teich J.:

ReProVide: Query Optimisation and Near-Data Processing on Reconfigurable SoCs for Big Data Analysis

21st Conference on Database Systems for Business, Technology and Web (Bamberg, 3. März 2025 - 7. März 2025)

In: **Proceedings of the 21st Conference on Database Systems for Business, Technology and Web 2025**

DOI: [10.18420/BTW2025-57](https://doi.org/10.18420/BTW2025-57)

BibTeX: [Download](#)

- Hernandez Morales JJ., Hannig F., Teich J.:

A SIMD MAC RISC-V Extension with Approximate Multipliers for Accelerating CNN Inference in Tiny Embedded Devices

*38th GI/ITG International Conference on Architecture of Computing Systems
(Kiel, 22. April 2025 - 24. April 2025)*

In: Sven Tomforde, Christian Krupitzer, Stephane Vialle, Estela Suarez, and Thilo Pionteck (ed.): **Architecture of Computing Systems, 38th International Conference, ARCS 2025, Kiel, Germany, April 22–24, 2025, Proceedings 2025**

DOI: [10.1007/978-3-032-03281-2_12](https://doi.org/10.1007/978-3-032-03281-2_12)

URL: https://link.springer.com/chapter/10.1007/978-3-032-03281-2_12

BibTeX: [Download](#)

- Karim A., [Falk J.](#), Teich J.:

[Exploration of Clock and Power Gating Tradeoffs for the Design of Self-Powering Dataflow Networks](#)

28. Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV) (Rostock Warnemünde, 11. März 2025 - 12. März 2025)

In: VDE ITG; VDE/VDI GMM; GI (ed.): **Proceedings of the 28th Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen**, Berlin - Offenbach: 2025

BibTeX: [Download](#)

- Krüger P., Wildermann S., Teich J.:

[Breaking Confidentiality of XTS-AES Encrypted Data at Rest on Microprocessors using Electromagnetic Side-Channel Attacks](#)

IEEE International Symposium on Hardware Oriented Security and Trust (HOST) (San Jose, 5. Mai 2025 - 8. Mai 2025)

In: IEEE (ed.): **2025 IEEE International Symposium on Hardware Oriented Security and Trust (HOST) 2025**

DOI: [10.1109/HOST64725.2025.11050075](https://doi.org/10.1109/HOST64725.2025.11050075)

URL: <https://ieeexplore.ieee.org/document/11050075>

BibTeX: [Download](#)

- Lamberti P., Esper K., Spieck J., Velasco-Guillen RJ., Beckerle P., Teich J.:

[Enforcing Safety Requirements of a Knee Orthosis Using Finite State Machines](#)

2nd International Conference on Integrated Systems in Medical Technologies (ISMT) (Erlangen, 25. September 2024 - 26. September 2024)

In: **2024 2nd International Conference on Integrated Systems in Medical Technologies (ISMT) 2025**

DOI: [10.1109/ISMT62540.2024.10985961](https://doi.org/10.1109/ISMT62540.2024.10985961)

URL: <https://ieeexplore.ieee.org/document/10985961>

BibTeX: [Download](#)

- [Plagwitz P.](#), Hannig F., Teich J., Keszocze O.:

[DSL-based SNN Accelerator Design using Chisel](#)

In: **Microprocessors and Microsystems** 118 (2025), Article No.: 105187

ISSN: 0141-9331

DOI: [10.1016/j.micpro.2025.105187](https://doi.org/10.1016/j.micpro.2025.105187)

BibTeX: [Download](#)

- Sabih M., Abdo M., Hannig F., Teich J.:

[Beyond BNNs: Design and Acceleration of Sub-Bit Neural Networks using RISC-V Custom Functional Units](#)

In: **IEEE Embedded Systems Letters** 17 (2025), p. 329-332

ISSN: 1943-0663

DOI: [10.1109/LES.2025.3600565](https://doi.org/10.1109/LES.2025.3600565)

BibTeX: [Download](#)

- Sabih M., Abdo M., Hannig F., Teich J.:

[Beyond BNNs: Design and Acceleration of Sub-Bit Neural Networks Using RISC-V Custom Functional Units](#)

In: **IEEE Embedded Systems Letters** 17 (2025), p. 329-332

ISSN: 1943-0663

DOI: [10.1109/LES.2025.3600565](https://doi.org/10.1109/LES.2025.3600565)

BibTeX: [Download](#)

- Sesli B., Sabih M., Hannig F., Teich J.:

[Design of Machine Learning Accelerators as RISC-V Extensions using an Open Source Tool Flow](#)

International Conference on Computer Aided Design (ICCAD) (Munich, 26. Oktober 2025 - 30. Oktober 2025)

In: IEEE (ed.): **Proceedings of the International Conference on Computer Aided Design (ICCAD) 2025**

DOI: [10.1109/ICCAD66269.2025.11240834](https://doi.org/10.1109/ICCAD66269.2025.11240834)

URL: <https://ieeexplore.ieee.org/document/11240834>

BibTeX: [Download](#)

- Seum T., Krüger P., Wildermann S., Teich J.:
[Die Verwendung von Seitenkanalangriffen durch die Strafverfolgungsbehörden Impraktikabel oder ein mächtiges Werkzeug?](#)

In: **MultiMedia und Recht** (2025), p. 98-104

ISSN: 1434-596X

URL: <https://beck-online.beck.de/Bcid/Y-300-Z-MMR-B-2025-S-98-N-1>

BibTeX: [Download](#)

- Sixdenier PL., Deutel M., Teich J.:
[Early-Exit Neural Architecture Search for Energy-Harvesting Edge Computing](#)

2025 IEEE 18th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoc) (Singapore, 15. Dezember 2025 - 18. Dezember 2025)

In: **2025 IEEE 18th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoc) 2025**

DOI: [10.1109/MCSoc67473.2025.00066](https://doi.org/10.1109/MCSoc67473.2025.00066)

URL: <https://ieeexplore.ieee.org/document/11311064>

BibTeX: [Download](#)

- Sixdenier PL., Wildermann S., Arockiaraj J., Teich J.:
[WiP Paper: Utility-Aware Transmission of Sensor Data on Energy-Harvesting IoT Gateways](#)

22nd International Conference on Embedded Wireless Systems and Networks (EWSN 2025) (Leuven, Belgium, 22. September 2025 - 25. September 2025)

In: **22nd International Conference on Embedded Wireless Systems and Networks (EWSN 2025) 2025**

BibTeX: [Download](#)

- Spieck J., Walter D., Waschkeit J., Teich J.:
[Co-Design of Sustainable Embedded Systems-on-Chip](#)

Design, Automation & Test in Europe Conference (DATE) (Lyon, 31. März 2025 - 2. April 2025)

In: **Design, Automation and Test in Europe Conference 2025**

DOI: [10.23919/DATE64628.2025.10992914](https://doi.org/10.23919/DATE64628.2025.10992914)

BibTeX: [Download](#)

- Spieck J., Walter D., Waschkeit J., Teich J.:

[Co-Design of Systems-on-Chip for Sustainability](#)

NG-RES 2025: Sixth Workshop on Next Generation Real-Time Embedded Systems (Barcelona, Spain, 20. Januar 2025 - 22. Januar 2025)

DOI: [10.4230/OASlcs.NG-RES.2025.3](https://doi.org/10.4230/OASlcs.NG-RES.2025.3)

URL: <https://drops.dagstuhl.de/entities/document/10.4230/OASlcs.NG-RES.2025.3>

BibTeX: [Download](#)

- Tahoori M., Becker J., Henkel J., Kunz W., Schlichtmann U., Sigl G., Teich J., Wehn N.:

[Multi-Partner Project: Open-Source Design Tools for Co-Development of AI Algorithms and AI Chips: \(Initial Stage\)](#)

2025 Design, Automation and Test in Europe Conference, DATE 2025 (Lyon, 31. März 2025 - 2. April 2025)

In: **2025 Design, Automation & Test in Europe Conference (DATE) 2025**

DOI: [10.23919/DATE64628.2025.10992986](https://doi.org/10.23919/DATE64628.2025.10992986)

BibTeX: [Download](#)

- Tahoori M., Meyers V., Sadeghipour Roodsari M., Xu H., Becker J., Harbaum T., Frombach F., Höfer J., Sotiropoulos G., Henkel J., Demirdag Z., Khdr H., Nassar H., Schlichtmann U., Geier J., van Kempen P., Sigl G., Kögler S., Probst M., Teich J., Hannig F., Sabih M., Sesli B., Wehn N., Steiner L., Kunz W., Shelkamy Ali M.:

[Special Session – Hardware-Software Co-Design for Machine Learning Systems Made Open-Source](#)

International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) (Taipei, 28. September 2025 - 3. Oktober 2025)

In: ACM (ed.): **Proceedings of the International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) 2025**

DOI: [10.1145/3742873.3756928](https://doi.org/10.1145/3742873.3756928)

URL: <https://dl.acm.org/doi/10.1145/3742873.3756928>

BibTeX: [Download](#)

- Walter D., Brand M., [Heidorn C.](#), Witterauf M., Hannig F., Teich J.:
[Europractice activity report 2024](#)
(2025), p. 29-30
URL: https://europractice-ic.com/wp-content/uploads/2025/03/Europractice_ActivityReport2024_webversion.pdf
BibTeX: [Download](#)
(Techreport)
- Walter D., Halm M., Seidel D., Ghosh I., [Heidorn C.](#), Hannig F., Teich J.:
[Evaluation of CGRA Toolchains](#)
1st Workshop on Open Source Solutions for Massively Parallel Integrated Circuits (OSSMPIC) (Lyon, 31. März 2025 - 2. April 2025)
In: **In Proceedings of the 1st Workshop on Open Source Solutions for Massively Parallel Integrated Circuits (OSSMPIC) 2025**
DOI: [10.48550/arXiv.2502.19114](https://doi.org/10.48550/arXiv.2502.19114)
BibTeX: [Download](#)
- Wilbert N., Szymanski M., Wildermann S., Herzog H., Hoenig T., Teich J.:
[CHaOS: A Persistent Lightweight Cache Hybridization-aware OS](#)
38th GI/ITG International Conference on Architecture of Computing Systems (Kiel, 22. April 2025 - 24. April 2025)
BibTeX: [Download](#)
- Wildermann S., Wilbert N., Häberlein T., Teich J.:
[Self-powered Embedded Systems: The Role of Non-volatile Memory Technology in IoT Devices](#)
In: Gidon Ernst, Matthias Güdemann, Alexander Knapp, Florian Nafz, Frank Ortmeier, Hella Ponsar, Gerhard Schellhorn, Alexander Schiendorfer (ed.): **Go Where the Bugs Are: Essays Dedicated to Wolfgang Reif on the Occasion of His 65th Birthday**, Cham: Springer, 2025, p. 155-177 (Lecture Notes in Computer Science)
ISBN: 978-3-031-92195-7
DOI: [10.1007/978-3-031-92196-4_8](https://doi.org/10.1007/978-3-031-92196-4_8)
BibTeX: [Download](#)

2024

- Deutel M., Hannig F., Mutschler C., Teich J.:
[Fused-Layer CNNs for Memory-Efficient Inference on Microcontrollers](#)
Workshop on Machine Learning and Compression @ NeurIPS 2024 (Vancouver Convention Center, 10. Dezember 2024 - 15. Dezember 2024)
Open Access: <https://openreview.net/forum?id=2O8qbyxH6X>
BibTeX: [Download](#)
- Deutel M., Hannig F., Mutschler C., Teich J.:
[On-Device Training of Fully Quantized Deep Neural Networks on Cortex-M Microcontrollers](#)
In: **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems** 44 (2024), p. 1250 - 1261
ISSN: 0278-0070
DOI: [10.1109/TCAD.2024.3484354](https://doi.org/10.1109/TCAD.2024.3484354)
URL: <https://ieeexplore.ieee.org/document/10726519>
BibTeX: [Download](#)
- Esper K., Teich J.:
[History-Based Run-Time Requirement Enforcement of Non-Functional Properties on MPSoCs](#)
Fifth Workshop on Next Generation Real-Time Embedded Systems (NG-RES 2024) (Munich, 17. Januar 2024 - 19. Januar 2024)
In: Patrick Meumeu Yomsi, Stefan Wildermann (ed.): **Fifth Workshop on Next Generation Real-Time Embedded Systems (NG-RES 2024)**, Saarbrücken/Waldern: 2024
DOI: [10.4230/OASlcs.NG-RES.2024.4](https://doi.org/10.4230/OASlcs.NG-RES.2024.4)
URL: <https://drops.dagstuhl.de/entities/document/10.4230/OASlcs.NG-RES.2024.4>
BibTeX: [Download](#)
- Esper K., Wildermann S., Teich J.:
[Range-Based Run-time Requirement Enforcement of Non-Functional Properties on MPSoCs](#)
Design, Automation and Test in Europe Conference (Valencia, 25. März 2024 - 27. März 2024)

In: **Design, Automation & Test in Europe Conference & Exhibition, DATE 2024** 2024

DOI: [10.23919/DATE58400.2024.10546881](https://doi.org/10.23919/DATE58400.2024.10546881)

URL: <https://ieeexplore.ieee.org/document/10546881>

BibTeX: [Download](#)

- Groth S., Schmid M., Teich J., Hannig F.:

[**Estimating the Execution Time of CNN Inference on GPUs**](#)

27th Workshop on Methods and Description Languages for Modelling and Verification of Circuits and Systems (MBMV) (Kaiserslautern, 14. Februar 2024 - 15. Februar 2024)

In: **Proceedings of the 27th Workshop on Methods and Description Languages for Modelling and Verification of Circuits and Systems (MBMV) 2024**

BibTeX: [Download](#)

- Hahn T., Schüll D., Wildermann S., Teich J.:

[**ABACUS: ASIP-based Avro Schema-customizable Parser Acceleration on FPGAs**](#)

International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS) (Kielce, 3. April 2024 - 5. April 2024)

In: **IEEE Proceedings of the 27th International Symposium on Design and Diagnostics of Electronic Circuits & Systems 2024**

DOI: [10.1109/DDECS60919.2024.10508904](https://doi.org/10.1109/DDECS60919.2024.10508904)

BibTeX: [Download](#)

- Hahn T., Wildermann S., Teich J.:

[**JSON-CooP: A JSON Decompression/Parsing Co-Design for FPGAs**](#)

International Conference on Field-Programmable Logic and Applications (FPL) (Turin, 2. September 2024 - 6. September 2024)

In: **IEEE Proceedings of the 34th International Conference on Field-Programmable Logic and Applications 2024**

DOI: [10.1109/FPL64840.2024.00012](https://doi.org/10.1109/FPL64840.2024.00012)

BibTeX: [Download](#)

- [Heidorn C.](#), Hannig F., Riedelbauch D., Strohmeyer C., Teich J.:

[**Efficient Deployment of Neural Networks for Thermal Monitoring on AURIX TC3xx Microcontrollers**](#)

10th International Conference on Vehicle Technology and Intelligent Transport Systems (VEHITS) (Angers, 2. Mai 2024 - 4. Mai 2024)

DOI: [10.5220/0000186800003702](https://doi.org/10.5220/0000186800003702)

BibTeX: [Download](#)

- [Heidorn C.](#), Hannig F., Riedelbauch D., Strohmeyer C., Teich J.:
[OpTC – A Toolchain for Deployment of Neural Networks on AURIX TC3xx Microcontrollers](#)

In: **The Computing Research Repository (CoRR)**, 2024

DOI: [10.48550/arXiv.2404.15833](https://doi.org/10.48550/arXiv.2404.15833)

URL: <https://arxiv.org/abs/2404.15833>

BibTeX: [Download](#)

(online publication)

- [Heidorn C.](#), Hannig F., Riedelbauch D., Strohmeyer C., Teich J.:
[OpTC – A Toolchain for Deployment of Neural Networks on AURIX TC3xx Microcontrollers](#)

2024 Stuttgart International Symposium on Automotive and Engine Technology (Stuttgart, 2. Juli 2024 - 3. Juli 2024)

In: André Casal Kulzer, Hans-Christian Reuss, Andreas Wagner (ed.): **Proceeding of the 2024 Stuttgart International Symposium on Automotive and Engine Technology**, Wiesbaden: 2024

DOI: [10.1007/978-3-658-45018-2_4](https://doi.org/10.1007/978-3-658-45018-2_4)

BibTeX: [Download](#)

- [Heidorn C.](#), Sabih M., Meyerhöfer N., Schinabeck C., Teich J., Hannig F.:
[Hardware-Aware Evolutionary Explainable Filter Pruning for Convolutional Neural Networks](#)

In: **International Journal of Parallel Programming** 52 (2024), p. 40 - 58

ISSN: 0885-7458

DOI: [10.1007/s10766-024-00760-5](https://doi.org/10.1007/s10766-024-00760-5)

BibTeX: [Download](#)

- Karim A., [Falk J.](#), Schmidt D., Teich J.:
[Self-Powering Dataflow Networks – Concepts and Implementation](#)

22nd ACM-IEEE International Symposium on Formal Methods and Models for System Design (MEMOCODE) (Raleigh, NC, 3. Oktober 2024 - 4. Oktober 2024)

In: **Proceedings of the 22nd ACM-IEEE International Symposium on Formal Methods and Models for System Design (MEMOCODE) 2024**

DOI: [10.1109/MEMOCODE63347.2024.00013](https://doi.org/10.1109/MEMOCODE63347.2024.00013)

BibTeX: [Download](#)

- Krüger P., Wildermann S., Teich J.:
[**CRESTS: Chronology-based Reconstruction for Side-Channel Trace Segmentation for XTS-AES on Complex Targets**](#)
17th European Workshop on Systems Security (EuroSec) (Athen, 22. April 2024 - 22. April 2024)
In: Association for Computing Machinery (ACM) (ed.): **EUROSEC '24: Proceedings of the 17th European Workshop on System Security 2024**
DOI: [10.1145/3642974.3652286](https://doi.org/10.1145/3642974.3652286)
BibTeX: [Download](#)
- Letras M., [Falk J.](#), Teich J.:
[**Exploring Multi-Reader Buffers and Channel Placement during Dataflow Network Mapping to Heterogeneous Many-core Systems**](#)
In: **IEEE Access** 12 (2024), p. 39748-39769
ISSN: 2169-3536
DOI: [10.1109/ACCESS.2024.3375079](https://doi.org/10.1109/ACCESS.2024.3375079)
BibTeX: [Download](#)
- [Plagwitz P.](#), Hannig F., Teich J., Keszöcze O.:
[**Compiler-based Processor Network Generation for Neural Networks on FPGAs**](#)
27th Workshop on Methods and Description Languages for Modelling and Verification of Circuits and Systems (MBMV) (Kaiserslautern, 14. Februar 2024 - 15. Februar 2024)
In: **Proceedings of the 27th Workshop on Methods and Description Languages for Modelling and Verification of Circuits and Systems (MBMV) 2024**
BibTeX: [Download](#)
- [Plagwitz P.](#), Hannig F., Teich J., Keszöcze O.:
[**DSL-based SNN Accelerator Design using Chisel**](#)
27th Euromicro Conference Series on Digital System Design (DSD) (Paris, 27. August 2024 - 30. August 2024)

In: **Proceedings of the 27th Euromicro Conference on Digital Systems Design (DSD) 2024**

DOI: [10.1109/DSD64264.2024.00032](https://doi.org/10.1109/DSD64264.2024.00032)

BibTeX: [Download](#)

- [Plagwitz P.](#), Hannig F., Teich J., Keszöcze O.:
[SNN vs. CNN Implementations on FPGAs: An Empirical Evaluation](#)
20th International Symposium on Applied Reconfigurable Computing. Architectures, Tools, and Applications (ARC) (Aveiro, 20. März 2024 - 22. März 2024)
In: **Proceedings of the 20th International Symposium on Applied Reconfigurable Computing. Architectures, Tools, and Applications (ARC) 2024**
DOI: [10.1007/978-3-031-55673-9_1](https://doi.org/10.1007/978-3-031-55673-9_1)
BibTeX: [Download](#)
- Sabih M., Karim A., Wittmann J., Hannig F., Teich J.:
[Hardware/Software Co-Design of RISC-V Extensions for Accelerating Sparse DNNs on FPGAs](#)
International Conference on Field Programmable Technology (FPT) (Sydney, Australia, 10. Dezember 2024 - 12. Dezember 2024)
In: IEEE (ed.): **Proceedings of International Conference on Field Programmable Technology (FPT) 2024**
DOI: [10.1109/ICFPT64416.2024.11113397](https://doi.org/10.1109/ICFPT64416.2024.11113397)
BibTeX: [Download](#)
- Sabih M., Sesli B., Hannig F., Teich J.:
[Accelerating DNNs using Weight Clustering on RISC-V Custom Functional Units](#)
Conference on Design, Automation and Test in Europe (DATE) (Valencia, 25. März 2024 - 27. März 2024)
In: **Proceedings of the Conference on Design, Automation and Test in Europe (DATE) 2024**
BibTeX: [Download](#)
- Sixdenier PL., Wildermann S., Teich J.:
[GRES: Guaranteed Remaining Energy Scheduling of Energy-harvesting Sensors by Quality Adaptation](#)

Cyber-Physical Systems & Internet of Things 2024 (CPS&IoT'2024) (Budva, Montenegro, 11. Juni 2024 - 14. Juni 2024)

In: **Proceedings of the 13th Mediterranean Conference on Embedded Computing (MECO) 2024**

BibTeX: [Download](#)

- Spieck J., Wildermann S., Teich J.:

[A Scenario-Based DVFS-Aware Hybrid Application Mapping Methodology for MPSoCs](#)

In: **ACM Transactions on Design Automation of Electronic Systems (2024)**

ISSN: 1084-4309

DOI: [10.1145/3660633](https://doi.org/10.1145/3660633)

BibTeX: [Download](#)

- Walter D., Adamtschuk T., Hannig F., Teich J.:

[Analysis and Optimization of Block LU Decomposition for Execution on Tightly Coupled Processor Arrays](#)

35th IEEE International Conference on Application-specific Systems, Architectures and Processors (Hong Kong, 24. Juli 2024 - 26. Juli 2024)

In: **Proceedings of the IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP) 2024**

DOI: [10.1109/ASAP61560.2024.00029](https://doi.org/10.1109/ASAP61560.2024.00029)

URL: <https://ieeexplore.ieee.org/document/10631126>

BibTeX: [Download](#)

- Walter D., Brand M., [Heidorn C.](#), Witterauf M., Hannig F., Teich J.:

[ALPACA: An Accelerator Chip for Nested Loop Programs](#)

IEEE International Symposium on Circuits and Systems (ISCAS) (Singapore, 19. Mai 2024 - 22. Mai 2024)

In: **Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS) 2024**

DOI: [10.1109/ISCAS58744.2024.10558549](https://doi.org/10.1109/ISCAS58744.2024.10558549)

URL: <https://ieeexplore.ieee.org/document/10558549>

BibTeX: [Download](#)

- Wilbert N., Wildermann S., Teich J.:

[Hybrid Cache Design Under Varying Power Supply Stability - A Comparative](#)

Study

10th International Symposium on Memory Systems (Washington, D.C., 30. September 2024 - 3. Oktober 2024)

In: **MEMSYS '24: Proceedings of the International Symposium on Memory Systems 2024**

DOI: [10.1145/3695794.3695819](https://doi.org/10.1145/3695794.3695819)

BibTeX: [Download](#)

- Wilbert N., Wildermann S., Teich J.:

To Keep or Not to Keep - The Volatility of Replacement Policy Metadata in Hybrid Caches

2nd Workshop on Disruptive Memory Systems (Austin, TX, 3. November 2024 - 3. November 2024)

In: **Proceedings of the 2nd Workshop on Disruptive Memory Systems 2024**

DOI: [10.1145/3698783.3699381](https://doi.org/10.1145/3698783.3699381)

BibTeX: [Download](#)

2023

- Bosio A., Barbareschi M., Savino A., Han J., Teich J.:

Special Issue on Approximate Computing: Challenges, Methodologies, Algorithms, and Architectures for Dependable and Secure Systems

In: **IEEE Design & Test** 40 (2023), p. 5-7

ISSN: 2168-2356

DOI: [10.1109/MDAT.2022.3221909](https://doi.org/10.1109/MDAT.2022.3221909)

BibTeX: [Download](#)

- Deutel M., Woller P., Mutschler C., Teich J.:

Energy-efficient Deployment of Deep Learning Applications on Cortex-M based Microcontrollers using Deep Compression

Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen MBMV'23 (Freiburg, 23. März 2023 - 24. März 2023)

In: VDE (ed.): **MBMV 2023; 26th Workshop 2023**

Open Access: <https://arxiv.org/abs/2205.10369>

URL: <https://ieeexplore.ieee.org/document/10173060>

BibTeX: [Download](#)

- Esper K., Spieck J., Sixdenier PL., Wildermann S., Teich J.:
[**RAVEN: Reinforcement Learning for Generating Verifiable Run-time Requirement Enforcers for MPSoCs**](#)
Workshop on Next Generation Real-Time Embedded Systems Co-located with HiPEAC 2023 (Toulouse, 18. Januar 2023 - 18. Januar 2023)
In: **Fourth Workshop on Next Generation Real-Time Embedded Systems (NG-RES 2023)**, Dagstuhl, Germany: 2023
DOI: [10.4230/OASlcs.NG-RES.2023.7](https://doi.org/10.4230/OASlcs.NG-RES.2023.7)
URL: <https://drops.dagstuhl.de/opus/volltexte/2023/17738>
BibTeX: [Download](#)
- Esper K., Wildermann S., Teich J.:
[**Automatic Synthesis of FSMs for Enforcing Non-Functional Requirements on MPSoCs Using Multi-Objective Evolutionary Algorithms**](#)
In: **ACM Transactions on Design Automation of Electronic Systems 28** (2023), p. 1-20
ISSN: 1084-4309
DOI: [10.1145/3617832](https://doi.org/10.1145/3617832)
BibTeX: [Download](#)
- Hahn T., Schüll D., Wildermann S., Teich J.:
[**An FPGA Avro Parser Generator for Accelerated Data Stream Processing**](#)
2nd Workshop on Novel Data Management Ideas on Heterogeneous (Co-)Processors (NoDMC) (Dresden, 6. März 2023 - 10. März 2023)
In: **Proceedings of the 2nd Workshop on Novel Data Management Ideas on Heterogeneous (Co-)Processors (NoDMC) 2023**
DOI: [10.18420/BTW2023-46](https://doi.org/10.18420/BTW2023-46)
BibTeX: [Download](#)
- Hahn T., Wildermann S., Teich J.:
[**SPEAR-JSON: Selective parsing of JSON to enable accelerated stream processing on FPGAs**](#)
International Conference on Field-Programmable Logic and Applications (FPL) (Göteborg, 4. September 2023 - 8. September 2023)
In: **IEEE Proceedings of the 33rd International Conference on Field-Programmable Logic and Applications 2023**

DOI: [10.1109/FPL60245.2023.00034](https://doi.org/10.1109/FPL60245.2023.00034)

BibTeX: [Download](#)

- Henkel J., Sidduh L., Bauer L., Teich J., Wildermann S., Tahoori MB., Mayahinia M., Castrillon J., Khan AA., Farzaneh H., de Lima JPC., Chen JJ., Hakert C., Chen KH., Yang CL., Cheng HY.:

[Special Session - Non-Volatile Memories: Challenges and Opportunities for Embedded System Architectures with Focus on Machine Learning Applications](#)

International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES) (HAMBURG, 18. September 2023 - 20. September 2023)

In: **Proceedings of the International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES) 2023**

BibTeX: [Download](#)

- Letras M., [Falk J.](#), Teich J.:

[Throughput and Memory Optimization for Parallel Implementations of Dataflow Networks using Multi-Reader Buffers](#)

Fourth Workshop on Next Generation Real-Time Embedded Systems (Toulouse, 18. Januar 2023 - 18. Januar 2023)

In: **Fourth Workshop on Next Generation Real-Time Embedded Systems (NG-RES 2023)**, Germany: 2023

DOI: [10.4230/OASlcs.NG-RES.2023.6](https://doi.org/10.4230/OASlcs.NG-RES.2023.6)

URL: <https://drops.dagstuhl.de/opus/volltexte/2023/17737/>

BibTeX: [Download](#)

- [Plagwitz P.](#), Hannig F., Teich J., Keszöcze O.:

[To Spike or Not to Spike? A Quantitative Comparison of SNN and CNN FPGA Implementations](#)

(2023)

Open Access: <https://arxiv.org/abs/2306.12742>

URL: <https://arxiv.org/abs/2306.12742>

BibTeX: [Download](#)

(online publication)

- Pradhan C., Letras M., Teich J.:

[Efficient Table-based Function Approximation on FPGAs using Interval](#)

[Splitting and BRAM Instantiation](#)

In: **ACM Transactions on Embedded Computing Systems** 22 (2023), p. 1-24

ISSN: 1539-9087

DOI: [10.1145/3580737](https://doi.org/10.1145/3580737)

BibTeX: [Download](#)

- Sabih M., Yayla M., Hannig F., Teich J., Chen JJ.:

[Robust and Tiny Binary Neural Networks using Gradient-based Explainability Methods](#)

EuroMLSys '23: Proceedings of the 3rd Workshop on Machine Learning and Systems (Rome, Italy, 8. Mai 2023 - 8. Mai 2023)

In: Eiko Yoneki, Luigi Nardi (ed.): **EuroMLSys '23: Proceedings of the 3rd Workshop on Machine Learning and System**, New York(NY) United States: 2023

DOI: [10.1145/3578356.3592595](https://doi.org/10.1145/3578356.3592595)

URL: <https://dl.acm.org/doi/10.1145/3578356.3592595>

BibTeX: [Download](#)

- Sixdenier PL., Wildermann S., Ottens M., Teich J.:

[Seque: Lean and Energy-aware Data Management for IoT Gateways](#)

IEEE International Conference on Edge Computing and Communications (EDGE) (Chicago, Illinois USA, 2. Juli 2023 - 8. Juli 2023)

DOI: [10.1109/EDGE60047.2023.00030](https://doi.org/10.1109/EDGE60047.2023.00030)

BibTeX: [Download](#)

- Spieck J., Sixdenier PL., Esper K., Wildermann S., Teich J.:

[Hybrid Genetic Reinforcement Learning for Generating Run-Time Requirement Enforcers](#)

21st ACM-IEEE International Symposium on Formal Methods and Models for System Design (MEMOCODE) (Hamburg, 21. September 2023 - 23. September 2023)

In: **2023 21st ACM-IEEE International Symposium on Formal Methods and Models for System Design (MEMOCODE) 2023**

DOI: [10.1145/3610579.3611091](https://doi.org/10.1145/3610579.3611091)

BibTeX: [Download](#)

- Spieck J., Wildermann S., Teich J.:
[**A Learning-Based Methodology for Scenario-Aware Mapping of Soft Real-Time Applications onto Heterogeneous MPSoCs**](#)
In: **ACM Transactions on Design Automation of Electronic Systems** 28 (2023), p. 4:1 - 4:40
ISSN: 1084-4309
DOI: [10.1145/3529230](https://doi.org/10.1145/3529230)
BibTeX: [Download](#)
- Trautmann J., Krüger P., Becher A., Wildermann S., Teich J.:
[**Design, Calibration, and Evaluation of Real-Time Waveform Matching on an FPGA-based Digitizer at 10 GS/s**](#)
In: **ACM Transactions on Reconfigurable Technology and Systems** (2023), p. 1-27
ISSN: 1936-7406
DOI: [10.1145/3635719](https://doi.org/10.1145/3635719)
URL: <https://dl.acm.org/doi/10.1145/3635719>
BibTeX: [Download](#)

2022

- Anantharajaiah N., Asfour T., Bader M., Bauer L., Becker J., Bischof S., Brand M., Bungartz HJ., Eichler C., Esper K., [Falk J.](#), Fafous N., Freiling F., Fried A., Gerndt M., Glaß M., Gonzalez J., Hannig F., [Heidorn C.](#), Henkel J., Herkersdorf A., Herzog B., John J., Hönig T., Hundhausen F., Khdr H., Langer T., Lenke O., Lesniak F., Lindermayr A., Listl A., Maier S., Megow N., Mettler M., Müller-Gritschneider D., Nassar H., Paus F., Pöppl A., Pourmohseni B., Rabenstein J., Raff-eck P., Rapp M., Rivas SN., Sagi M., Schirmacher F., Schlichtmann U., Schmaus F., Schröder-Preikschat W., Schwarzer T., Sikal MB., Simon B., Snelting G., Spieck J., Srivatsa A., Stechele W., Teich J., Comprés Ureña IA., Verbauwhede I., Walter D., Wild T., Wildermann S., Wille M., Witterauf M., Zhang L.:
[**Invasive Computing**](#)
FAU University Press, 2022
ISBN: 978-3-96147-571-1

DOI: [10.25593/978-3-96147-571-1](https://doi.org/10.25593/978-3-96147-571-1)

BibTeX: [Download](#)

- Brand M., Keszöcze O., Teich J.:

[Precision- and Accuracy-Reconfigurable Processor Architectures—An Overview](#)

In: **IEEE Transactions on Circuits and Systems II: Express Briefs** 69 (2022),
p. 2661 - 2666

ISSN: 1057-7130

DOI: [10.1109/TCSII.2022.3173753](https://doi.org/10.1109/TCSII.2022.3173753)

BibTeX: [Download](#)

- Brand P., Hackenberg B., [Falk J.](#), Teich J.:

[Grant Prediction-based Dynamic Power Management for 5G to Reduce Mobile Device Energy Consumption](#)

International Wireless Communications and Mobile Computing Conference (IWCMC 2022) (Dubrovnik)

DOI: [10.1109/iwcmc55113.2022.9824349](https://doi.org/10.1109/iwcmc55113.2022.9824349)

BibTeX: [Download](#)

- Echavarria Gutiérrez JA., Keszöcze O., Teich J.:

[Probability-based DSE of Approximated LUT-based FPGA Designs](#)

15th IEEE Dallas Circuits and Systems Conference (Dallas, 17. Juni 2022 - 19. Juni 2022)

DOI: [10.1109/dcas53974.2022.9845591](https://doi.org/10.1109/dcas53974.2022.9845591)

BibTeX: [Download](#)

- Echavarria Gutiérrez JA., Wildermann S., Keszöcze O., Khosravi F., Becher A., Teich J.:

[Design and Error Analysis of Accuracy-configurable Sequential Multipliers via Segmented Carry Chains](#)

In: **it - Information Technology** (2022)

ISSN: 1611-2776

DOI: [10.1515/itit-2021-0040](https://doi.org/10.1515/itit-2021-0040)

BibTeX: [Download](#)

- Esper K., Wildermann S., Teich J.:

[Multi-requirement Enforcement of Non-Functional Properties on MPSoCs](#)

[Using Enforcement FSMs - A Case Study](#)

Workshop on Next Generation Real-Time Embedded Systems (NG-RES) (Budapest, 22. Juni 2022 - 22. Juni 2022)

In: **Third Workshop on Next Generation Real-Time Embedded Systems (NG-RES 2022)**, Dagstuhl, Germany: 2022

DOI: [10.4230/OASlcs.NG-RES.2022.2](https://doi.org/10.4230/OASlcs.NG-RES.2022.2)

URL: <https://drops.dagstuhl.de/opus/volltexte/2022/16110/>

BibTeX: [Download](#)

- Hahn T., Becher A., Wildermann S., Teich J.:

[Raw Filtering of JSON data on FPGAs](#)

Design, Automation and Test in Europe Conference (DATE) (Antwerpen, 14. März 2022 - 23. März 2022)

In: **Proceedings of the 2022 Conference & Exhibition on Design, Automation & Test in Europe 2022**

DOI: [10.23919/DATE54114.2022.9774696](https://doi.org/10.23919/DATE54114.2022.9774696)

BibTeX: [Download](#)

- Hahn T., Wildermann S., Teich J.:

[Auto-Tuning of Raw Filters for FPGAs](#)

International Conference on Field-Programmable Logic and Applications (FPL) (Belfast, United Kingdom, 29. August 2022 - 2. September 2022)

In: **IEEE Proceedings of the 32nd International Conference on Field-Programmable Logic and Applications 2022**

DOI: [10.1109/FPL57034.2022.00036](https://doi.org/10.1109/FPL57034.2022.00036)

BibTeX: [Download](#)

- [Heidorn C.](#), Meyerhöfer N., Schinabeck C., Hannig F., Teich J.:

[Hardware-Aware Evolutionary Filter Pruning](#)

International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS XXII) (Pythagoreio, Samos, 3. Juli 2022 - 7. Juli 2022)

DOI: [10.1007/978-3-031-15074-6_18](https://doi.org/10.1007/978-3-031-15074-6_18)

BibTeX: [Download](#)

- Mishra A., Hannig F., Teich J., Sabih M.:

[MOSP: Multi-Objective Sensitivity Pruning of Deep Neural Networks](#)

*The 13th International Green and Sustainable Computing Conference (IGSC)
(Virtual, 24. Oktober 2022 - 27. Oktober 2022)*

In: IEEE (ed.): **2022 IEEE 13th International Green and Sustainable Computing Conference (IGSC)**, Pittsburgh, PA, USA: 2022

DOI: [10.1109/IGSC55832.2022.9969363](https://doi.org/10.1109/IGSC55832.2022.9969363)

URL: <https://ieeexplore.ieee.org/document/9969374>

BibTeX: [Download](#)

- [Plagwitz P.](#), Hannig F., Teich J.:

[TRAC: Compilation-based Design of Transformer Accelerators for FPGAs](#)

*International Conference on Field Programmable Logic and Applications (FPL)
(Belfast, United Kingdom, 29. August 2022 - 2. September 2022)*

In: **IEEE Proceedings of the 32nd International Conference on Field Programmable Logic and Applications 2022**

DOI: [10.1109/FPL57034.2022.00015](https://doi.org/10.1109/FPL57034.2022.00015)

BibTeX: [Download](#)

- Pourmohseni B., Wildermann S., Smirnov F., Meyer P., Teich J.:

[Task Migration Policy for Thermal-Aware Dynamic Performance Optimization in Many-Core Systems](#)

In: **IEEE Access** (2022)

ISSN: 2169-3536

DOI: [10.1109/ACCESS.2022.3162617](https://doi.org/10.1109/ACCESS.2022.3162617)

BibTeX: [Download](#)

- Sabih M., Hannig F., Teich J.:

[DyFiP: Explainable AI-based Dynamic Filter Pruning of Convolutional Neural Networks](#)

2nd European Workshop on Machine Learning and Systems (EuroMLSys) (Rennes, France, 5. April 2022 - 8. April 2022)

In: **Proceedings of the 2nd European Workshop on Machine Learning and Systems (EuroMLSys)**, New York, NY, United States: 2022

DOI: [10.1145/3517207.3526982](https://doi.org/10.1145/3517207.3526982)

BibTeX: [Download](#)

- Sixdenier PL., Wildermann S., Ziegler D., Teich J.:

[SIDAM: A Design Space Exploration Framework for Multi-Sensor Embedded](#)

[Systems Powered by Energy Harvesting](#)

International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS XXII) (Pythagoreio, Samos, 3. Juli 2022 - 7. Juli 2022)

In: Springer, Cham (ed.): **International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS XXII)**, Switzerland: 2022

DOI: [10.1007/978-3-031-15074-6](https://doi.org/10.1007/978-3-031-15074-6)

BibTeX: [Download](#)

- Snelting G., Teich J., Fried A., Hannig F., Witterauf M.:

[Compilation and Code Generation for Invasive Programs](#)

In: Jürgen Teich, Jörg Henkel, Andreas Herkersdorf (ed.): **Invasive Computing**, FAU University Press, 2022, p. 309-333

ISBN: 978-3-96147-571-1

DOI: [10.25593/978-3-96147-571-1](https://doi.org/10.25593/978-3-96147-571-1)

BibTeX: [Download](#)

- Sommer J., Özkan MA., Keszöcze O., Teich J.:

[DSP-Packing: Squeezing Low-precision Arithmetic into FPGA DSP Blocks](#)

International Conference on Field Programmable Logic and Applications (FPL) (Belfast, United Kingdom, 29. August 2022 - 2. September 2022)

In: **IEEE Proceedings of the 32nd International Conference on Field Programmable Logic and Applications 2022**

DOI: [10.1109/FPL57034.2022.00035](https://doi.org/10.1109/FPL57034.2022.00035)

BibTeX: [Download](#)

- Sommer J., Özkan MA., Keszöcze O., Teich J.:

[Efficient Hardware Acceleration of Sparsely Active Convolutional Spiking Neural Networks](#)

In: **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems** 41 (2022), p. 3767 - 3778

ISSN: 0278-0070

DOI: [10.1109/TCAD.2022.3197512](https://doi.org/10.1109/TCAD.2022.3197512)

BibTeX: [Download](#)

- Sommer J., Özkan MA., Keszöcze O., Teich J.:
[Efficient Hardware Acceleration of Sparsely Active Convolutional Spiking Neural Networks](#)
International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) (Shanghai, 7. Oktober 2022 - 14. Oktober 2022)
DOI: [10.1109/tcad.2022.3197512](https://doi.org/10.1109/tcad.2022.3197512)
BibTeX: [Download](#)
- Spieck J., Wildermann S., Teich J.:
[On Transferring Application Mapping Knowledge Between Differing MPSoC Architectures](#)
CODES+ISSS 2022 (Shanghai, 10. Oktober 2022 - 12. Oktober 2022)
In: **CODES+ISSS 2022** 2022
DOI: [10.1109/TCAD.2022.3197527](https://doi.org/10.1109/TCAD.2022.3197527)
BibTeX: [Download](#)
- Teich J., Brand M., Hannig F., [Heidorn C.](#), Walter D., Witterauf M.:
[Invasive Tightly-Coupled Processor Arrays](#)
In: Jürgen Teich, Jörg Henkel, Andreas Herkersdorf (ed.): **Invasive Computing**, FAU University Press, 2022, p. 177-202
ISBN: 978-3-96147-571-1
DOI: [10.25593/978-3-96147-571-1](https://doi.org/10.25593/978-3-96147-571-1)
BibTeX: [Download](#)
- Teich J., Esper K., [Falk J.](#), Pourmohseni B., Schwarzer T., Wildermann S.:
[Basics of Invasive Computing](#)
In: Jürgen Teich, Jörg Henkel, Andreas Herkersdorf (ed.): **Invasive Computing**, FAU University Press, 2022, p. 69-95
ISBN: 978-3-96147-571-1
DOI: [10.25593/978-3-96147-571-1](https://doi.org/10.25593/978-3-96147-571-1)
BibTeX: [Download](#)
- Teich J., Henkel J., Herkersdorf A.:
[Introduction to Invasive Computing](#)
In: Jürgen Teich, Jörg Henkel, Andreas Herkersdorf (ed.): **Invasive Computing**, FAU University Press, 2022, p. 1-66
ISBN: 978-3-96147-571-1

DOI: [10.25593/978-3-96147-571-1](https://doi.org/10.25593/978-3-96147-571-1)

BibTeX: [Download](#)

- Trautmann J., Beckers A., Wouters L., Gierlichs B., Wildermann S., Verbauwhede I., Teich J.:

[Semi-Automatic Locating of Cryptographic Operations in Side-Channel Traces](#)

CHES 2022 (Leuven, Belgium, 18. September 2022 - 21. September 2022)

In: **IACR Transactions on Cryptographic Hardware and Embedded Systems (TCHES) 2022**

DOI: [10.46586/tches.v2022.i1.345-366](https://doi.org/10.46586/tches.v2022.i1.345-366)

BibTeX: [Download](#)

- Trautmann J., Patsiatzis N., Becher A., Teich J., Wildermann S.:

[Real-Time Waveform Matching with a Digitizer at 10 GS/s](#)

International Conference on Field Programmable Logic and Applications (FPL) (Belfast, United Kingdom, 29. August 2022 - 2. September 2022)

In: **IEEE Proceedings of the 32nd International Conference on Field Programmable Logic and Applications 2022**

DOI: [10.1109/FPL57034.2022.00025](https://doi.org/10.1109/FPL57034.2022.00025)

URL: <https://ieeexplore.ieee.org/document/10035208>

BibTeX: [Download](#)

- Trautmann J., Patsiatzis N., Becher A., Wildermann S., Teich J.:

[Putting IMT to the Test: Revisiting and Expanding Interval Matching Techniques and their Calibration for SCA](#)

ASHES 2022 (Los Angeles, CA, USA, 11. November 2022 - 11. November 2022)

In: Association for Computing Machinery (ed.): **Proceedings of the 2022 Workshop on Attacks and Solutions in Hardware Security 2022**

DOI: [10.1145/3560834.3563828](https://doi.org/10.1145/3560834.3563828)

URL: <https://dl.acm.org/doi/10.1145/3560834.3563828>

BibTeX: [Download](#)

- Trautmann J., Teich J., Wildermann S.:

[Characterization of Side Channels on FPGA-based Off-The-Shelf Boards against Automated Attacks](#)

30th IEEE International Symposium on Field-Programmable Custom Computing

Machines (New York City, 15. Mai 2022 - 18. Mai 2022)

In: **30th IEEE International Symposium on Field-Programmable Custom Computing Machines 2022**

DOI: [10.1109/FCCM53951.2022.9786190](https://doi.org/10.1109/FCCM53951.2022.9786190)

BibTeX: [Download](#)

2021

- Alhaddad S., Förstner J., Groth S., Grünewald D., Grynko Y., Hannig F., Kenter T., Pfreundt F.J., Plessl C., Schotte M., Steinke T., Teich J., Weiser M., Wende F.:
[HighPerMeshes -- A Domain-Specific Language for Numerical Algorithms on Unstructured Grids](#)
18th International Workshop on Algorithms, Models and Tools for Parallel Computing on Heterogeneous Platforms (HeteroPar) (Warsaw, 24. August 2020 - 24. August 2020)
In: **Proceedings of the 18th International Workshop on Algorithms, Models and Tools for Parallel Computing on Heterogeneous Platforms (HeteroPar) in Euro-Par 2020: Parallel Processing Workshops 2021**
DOI: [10.1007/978-3-030-71593-9_15](https://doi.org/10.1007/978-3-030-71593-9_15)
BibTeX: [Download](#)
- Alhaddad S., Förstner J., Groth S., Grünewald D., Grynko Y., Hannig F., Kenter T., Pfreundt F.J., Plessl C., Schotte M., Steinke T., Teich J., Weiser M., Wende F.:
[The HighPerMeshes Framework for Numerical Algorithms on Unstructured Grids](#)
In: **Concurrency and Computation-Practice & Experience** (2021)
ISSN: 1532-0626
DOI: [10.1002/cpe.6616](https://doi.org/10.1002/cpe.6616)
BibTeX: [Download](#)
- Beena Gopalakrishnan Nair L., Becher A., Wildermann S., Meyer-Wegener K., Teich J.:
[Speculative Dynamic Reconfiguration and Table Prefetching Using Query Look-Ahead in the ReProVide Near-Data-Processing System](#)
In: **Datenbank-Spektrum** (2021)
ISSN: 1618-2162

DOI: [10.1007/s13222-020-00363-7](https://doi.org/10.1007/s13222-020-00363-7)

URL: <https://rd.springer.com/article/10.1007/s13222-020-00363-7>

BibTeX: [Download](#)

- Bosio A., O'Connor I., Traiola M., Echavarria Gutiérrez JA., Teich J., Abdullah Hanif M., Shafique M., Hamdioui S., Deveautour B., Girard P., Virazel A., Bertels K.:
[Emerging Computing Devices: Challenges and Opportunities for Test and Reliability*](#)
IEEE European Test Symposium (ETS) (Virtual Conference, 24. Mai 2021 - 28. Mai 2021)
In: **Proceedings of the 26th IEEE European Test Symposium (ETS) 2021**
DOI: [10.1109/ETS50041.2021.9465409](https://doi.org/10.1109/ETS50041.2021.9465409)
BibTeX: [Download](#)
- Brand P., [Falk J.](#), Ah Sue J., Brendel J., Hasholzner R., Teich J.:
[Adaptive Predictive Power Management for Mobile LTE Devices](#)
In: **IEEE Transactions on Mobile Computing** 20 (2021), p. 2518-2535
ISSN: 1536-1233
DOI: [10.1109/TMC.2020.2988651](https://doi.org/10.1109/TMC.2020.2988651)
BibTeX: [Download](#)
- Brand P., [Falk J.](#), Maier T., Teich J.:
[Simulating Realistic IoT Network Traffic Using Similarity-based DSE](#)
International Conference on Computational Science and Computational Intelligence (CSCI) (Las Vegas, NV)
In: **2021 International Conference on Computational Science and Computational Intelligence (CSCI)**, New York: 2021
DOI: [10.1109/CSCI54926.2021.00276](https://doi.org/10.1109/CSCI54926.2021.00276)
BibTeX: [Download](#)
- Brand P., [Falk J.](#), Potwigin E., Teich J.:
[Multi-Step Ahead Grant Prediction for Dynamic Power Management in Cellular Modems](#)
2021 International Symposium on Networks, Computers and Communications (ISNCC 2021) (Canadian University, Citywalk, Dubai, 31. Oktober 2021 - 2. November 2021)

In: IEEE (ed.): **Proceedings of the 2021 International Symposium on Networks, Computers and Communications (ISNCC 2021)** 2021

DOI: [10.1109/ISNCC52172.2021.9615819](https://doi.org/10.1109/ISNCC52172.2021.9615819)

BibTeX: [Download](#)

- Echavarria Gutiérrez JA., Wildermann S., Keszöcze O., Khosravi F., Becher A., Teich J.:

[On the Approximation of Accuracy-configurable Sequential Multipliers via Segmented Carry Chains](#)

(2021)

URL: <http://arxiv.org/abs/2105.05588>

BibTeX: [Download](#)

(online publication)

- Echavarria Gutiérrez JA., Wildermann S., Teich J.:

[Approximate Logic Synthesis of Very Large Boolean Networks](#)

Design, Automation and Test in Europe, DATE 2021, February 1-5, 2021 (AI-pepxo, Grenoble, 1. Februar 2021 - 5. Februar 2021)

In: **Design, Automation and Test in Europe, DATE 2021** 2021

DOI: [10.23919/date51398.2021.9473952](https://doi.org/10.23919/date51398.2021.9473952)

BibTeX: [Download](#)

- Esper K., Wildermann S., Teich J.:

[A Comparative Evaluation of Latency-Aware Energy Optimization Approaches in Many-Core Systems](#)

Workshop on Next Generation Real-Time Embedded Systems (NG-RES) (Budapest, 20. Januar 2021 - 20. Januar 2021)

In: **Proceedings of the Workshop on Next Generation Real-Time Embedded Systems (NG-RES), OASICS Vol. 87** 2021

DOI: [10.4230/OASICS.NG-RES.2021.1](https://doi.org/10.4230/OASICS.NG-RES.2021.1)

URL: <https://drops.dagstuhl.de/opus/volltexte/2021/13477>

BibTeX: [Download](#)

- Esper K., Wildermann S., Teich J.:

[Enforcement FSMs - Specification and Verification of Non-Functional Properties of Program Executions on MPSoCs](#)

19th ACM-IEEE International Conference on Formal Methods and Models for

System Design (MEMOCODE'21) (Beijing, 20. November 2021 - 22. November 2021)

In: **Proceedings of the 19th ACM-IEEE International Conference on Formal Methods and Models for System Design**, New York, NY, USA: 2021

DOI: [10.1145/3487212.3487348](https://doi.org/10.1145/3487212.3487348)

BibTeX: [Download](#)

- Groth S., Teich J., Hannig F.:

[Efficient Application of Tensor Core Units for Convolving Images](#)

24th International Workshop on Software and Compilers for Embedded Systems (Eindhoven (NL), 1. November 2021 - 2. November 2021)

In: **Proceedings of the 24th International Workshop on Software and Compilers for Embedded Systems 2021**

DOI: [10.1145/3493229.3493305](https://doi.org/10.1145/3493229.3493305)

BibTeX: [Download](#)

- Hannig F., Teich J.:

[Open Source Hardware](#)

In: **IEEE Computer** 54 (2021), p. 111-115

ISSN: 0018-9162

DOI: [10.1109/MC.2021.3099046](https://doi.org/10.1109/MC.2021.3099046)

BibTeX: [Download](#)

- [Heidorn C.](#), Walter D., Candir YE., Hannig F., Teich J.:

[Hand Sign Recognition via Deep Learning on Tightly Coupled Processor Arrays](#)

31st International Conference on Field Programmable Logic and Applications (FPL) (Virtual Conference, 30. August 2021 - 3. September 2021)

In: **Proceedings of the 31st International Conference on Field Programmable Logic and Applications (FPL) 2021**

DOI: [10.1109/FPL53798.2021.00079](https://doi.org/10.1109/FPL53798.2021.00079)

BibTeX: [Download](#)

- Keszöcze O., Brand M., Witterauf M., [Heidorn C.](#), Teich J.:

[Aarith: An Arbitrary Precision Number Library](#)

ACM/SIGAPP Symposium On Applied Computing (virtual conference, 22. März 2021 - 26. März 2021)

DOI: [10.1145/3412841.3442085](https://doi.org/10.1145/3412841.3442085)

BibTeX: [Download](#)

- Khosravi F., Raß A., Teich J.:

[Efficient Computation of Probabilistic Dominance in Multi-objective Optimization](#)

In: **ACM Transactions on Evolutionary Learning and Optimization 1** (2021),
p. 1-26

ISSN: 2688-299X

DOI: [10.1145/3469801](https://doi.org/10.1145/3469801)

BibTeX: [Download](#)

- Letras M., [Falk J.](#), Teich J.:

[Decision Tree-based Throughput Estimation to Accelerate Design Space Exploration for Multi-Core Applications](#)

24. Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (München, 18. März 2021 - 19. März 2021)

BibTeX: [Download](#)

- [Plagwitz P.](#), Hannig F., Ströbel M., Strohmeier C., Teich J.:

[A Safari through FPGA-based Neural Network Compilation and Design Automation Flows](#)

29th IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM) (Virtual Conference, 9. Mai 2021 - 12. Mai 2021)

In: **Proceedings of the 29th IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM) 2021**

DOI: [10.1109/FCCM51124.2021.00010](https://doi.org/10.1109/FCCM51124.2021.00010)

URL: <https://ieeexplore.ieee.org/document/9444092>

BibTeX: [Download](#)

- Qiao B., Teich J., Hannig F.:

[An Efficient Approach for Image Border Handling on GPUs via Iteration Space Partitioning](#)

2021 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW) (Portland, OR, 17. Mai 2021 - 21. Mai 2021)

In: **Proceedings of the 2021 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW) 2021**

DOI: [10.1109/IPDPSW52791.2021.00067](https://doi.org/10.1109/IPDPSW52791.2021.00067)

BibTeX: [Download](#)

- Sabih M., Hannig F., Teich J.:

[**Fault-Tolerant Low-Precision DNNs using Explainable AI**](#)

Workshop on Dependable and Secure Machine Learning (DSML) (Virtual Workshop, 21. Juni 2021 - 24. Juni 2021)

In: **2021 51st Annual IEEE/IFIP International Conference on Dependable Systems and Networks Workshops (DSN-W) 2021**

DOI: [10.1109/DSN-W52860.2021.00036](https://doi.org/10.1109/DSN-W52860.2021.00036)

URL: <https://ieeexplore.ieee.org/document/9502445/>

BibTeX: [Download](#)

- Schlumberger J., Wildermann S., Teich J.:

[**CORSICA: A Framework for Conducting Real-World Side-Channel Analysis**](#)

In: IEEE (ed.): **2nd IFIP NTMS Workshop on CyberSecurity on Hardware 2021 (CyberSECHARD'21)**, 2021, p. 1-5

DOI: [10.1109/NTMS49979.2021.9432644](https://doi.org/10.1109/NTMS49979.2021.9432644)

BibTeX: [Download](#)

- Schuster A., [Heidorn C.](#), Brand M., Keszöcze O., Teich J.:

[**Design Space Exploration of Time, Energy, and Error Rate Trade-offs for CNNs using Accuracy-Programmable Instruction Set Processors**](#)

2nd International Workshop on IoT, Edge, and Mobile for Embedded Machine Learning (ITEM) (Virtual Event, 13. September 2021 - 17. September 2021)

In: Springer, Cham (ed.): **Joint European Conference on Machine Learning and Principles and Practice of Knowledge Discovery in Databases (ECML PKDD 2021)**, Switzerland: 2021

DOI: [10.1007/978-3-030-93736-2_29](https://doi.org/10.1007/978-3-030-93736-2_29)

BibTeX: [Download](#)

- Smirnov F., Pourmohseni B., Glaß M., Teich J.:

[**Efficient Symbolic Routing Encoding for In-vehicle Network Optimization**](#)

In: **Smart Cities, Green Technologies and Intelligent Transport Systems**, Springer, 2021, p. 173 - 199

ISBN: 978-3-030-68028-2

DOI: [10.1007/978-3-030-68028-2_9](https://doi.org/10.1007/978-3-030-68028-2_9)

URL: https://link.springer.com/chapter/10.1007/978-3-030-68028-2_9

BibTeX: [Download](#)

- Spieck J., Wildermann S., Teich J.:
[**Domain-Adaptive Soft Real-Time Hybrid Application Mapping for MPSoCs**](#)
3rd ACM/IEEE Workshop on Machine Learning for CAD (MLCAD) (North Carolina State University, Raleigh, NC, USA & Online, 31. August 2021 - 2. September 2021)
In: **3rd ACM/IEEE Workshop on Machine Learning for CAD (MLCAD) 2021**
DOI: [10.1109/MLCAD52597.2021.9531269](https://doi.org/10.1109/MLCAD52597.2021.9531269)
BibTeX: [Download](#)
- Streit FJ., Krüger P., Becher A., Schlumberger J., Wildermann S., Teich J.:
[**CHOICE – A Tunable PUF-Design for FPGAs**](#)
International Conference on Field-Programmable Logic and Applications (FPL) (Dresden, Germany, 30. August 2021 - 3. September 2021)
In: **IEEE Proceedings of the 31th International Conference on Field Programmable Logic and Applications 2021**
DOI: [10.1109/FPL53798.2021.00015](https://doi.org/10.1109/FPL53798.2021.00015)
BibTeX: [Download](#)
- Streit FJ., Krüger P., Becher A., Wildermann S., Teich J.:
[**Design and Evaluation of a Tunable PUF Architecture for FPGAs**](#)
In: **ACM Transactions on Reconfigurable Technology and Systems 15** (2021), p. 1-27
ISSN: 1936-7406
DOI: [10.1145/3491237](https://doi.org/10.1145/3491237)
BibTeX: [Download](#)
- Streit FJ., Krüger P., Becher A., Wildermann S., Teich J.:
[**Design and Evaluation of a Tunable PUF Architecture for FPGAs**](#)
International Conference on Field-Programmable Technology (FPT) (Auckland, New Zealand, 6. Dezember 2021 - 10. Dezember 2021)
In: **IEEE Proceedings of the 20th International Conference on Field-Programmable Technology 2021**

DOI: [10.1109/ICFPT52863.2021](https://doi.org/10.1109/ICFPT52863.2021)

BibTeX: [Download](#)

- Streit F.J., Wildermann S., Pschyklenk M., Teich J.:
[**Providing Tamper-Secure SoC Updates through Reconfigurable Hardware**](#)
International Symposium on Applied Reconfigurable Computing (ARC) (Rennes, France, 29. Juni 2021 - 1. Juli 2021)
In: **Springer Proceedings of the 17th International Symposium on Applied Reconfigurable Computing 2021**
DOI: [10.1007/978-3-030-79025-7_17](https://doi.org/10.1007/978-3-030-79025-7_17)
BibTeX: [Download](#)
- Traiola M., Echavarria Gutiérrez JA., Bosio A., Teich J., O'Connor I.:
[**Design Space Exploration of Approximation-Based Quadruple Modular Redundancy Circuits**](#)
International Conference On Computer Aided Design (Virtual conference, 1. November 2021 - 4. November 2021)
In: **Proceedings of the International Conference on Computer-Aided Design, ICCAD 2021**
DOI: [10.1109/iccad51958.2021.9643561](https://doi.org/10.1109/iccad51958.2021.9643561)
BibTeX: [Download](#)
- Walter D., Teich J.:
[**LION: Real-Time I/O Transfer Control for Massively Parallel Processor Arrays**](#)
19th ACM-IEEE International Conference on Formal Methods and Models for System Design (Beijing, China, 20. November 2021 - 22. November 2021)
In: **Proceedings of the 19th ACM-IEEE International Conference on Formal Methods and Models for System Design (MEMOCODE) 2021**
DOI: [10.1145/3487212.3487349](https://doi.org/10.1145/3487212.3487349)
BibTeX: [Download](#)
- Witterauf M., Walter D., Hannig F., Teich J.:
[**Symbolic Loop Compilation for Tightly Coupled Processor Arrays**](#)
In: **ACM Transactions on Embedded Computing Systems (2021)**
ISSN: 1539-9087

DOI: [10.1145/3466897](https://doi.org/10.1145/3466897)

BibTeX: [Download](#)

- Özkan MA., Ok B., Qiao B., Teich J., Hannig F.:
[HipaccVX: Wedding of OpenVX and DSL-based Code Generation](#)
In: **Journal of Real-Time Image Processing** 18 (2021), p. 765 - 777
ISSN: 1861-8200
DOI: [10.1007/s11554-020-01015-5](https://doi.org/10.1007/s11554-020-01015-5)
URL: <http://link.springer.com/article/10.1007/s11554-020-01015-5>
BibTeX: [Download](#)

2020

- Aliee H., Glaß M., Khosravi F., Teich J.:
[Uncertainty-Aware Compositional System-Level Reliability Analysis](#)
In: Henkel, Jörg, Dutt, Nikil (ed.): **Dependable Embedded Systems**, 2020
ISBN: 978-3-030-52017-5
DOI: [10.1007/978-3-030-52017-5_19](https://doi.org/10.1007/978-3-030-52017-5_19)
BibTeX: [Download](#)
- Arvind TKR., Brand M., [Heidorn C.](#), Boppu S., Hannig F., Teich J.:
[Hardware Implementation of Hyperbolic Tangent Activation Function for Floating Point Formats](#)
24th International Symposium on VLSI Design and Test (VDAT) (Bhubaneswar, 23. Juli 2020 - 25. Juli 2020)
In: **Proceedings of the 24th International Symposium on VLSI Design and Test (VDAT) 2020**
DOI: [10.1109/VDAT50263.2020.9190305](https://doi.org/10.1109/VDAT50263.2020.9190305)
BibTeX: [Download](#)
- Beena Gopalakrishnan Nair L., Becher A., Meyer-Wegener K., Wildermann S., Teich J.:
[SQL Query Processing Using an Integrated FPGA-based Near-Data Accelerator in ReProVide](#)
23rd International Conference on Extending Database Technology (Copenhagen, 30. März 2020 - 2. April 2020)

In: **Proceedings of EDBT 2020**

BibTeX: [Download](#)

- Brand M., Witterauf M., Bosio A., Teich J.:

[Anytime Floating-Point Addition and Multiplication – Concepts and Implementations](#)

Conference on Application-specific Systems, Architectures and Processors (ASAP 2020) (Manchester, U.K., 6. Juli 2020 - 8. Juli 2020)

In: **Proceedings of the 31st IEEE International Conference on Application-specific Systems, Architectures and Processors 2020**

DOI: [10.1109/ASAP49362.2020.00034](https://doi.org/10.1109/ASAP49362.2020.00034)

BibTeX: [Download](#)

- Brand P., Sabih M., [Falk J.](#), Ah Sue J., Teich J.:

[Clustering-Based Scenario-Aware LTE Grant Prediction](#)

IEEE Wireless Communications and Networking Conference (WCNC2020) (Seoul, 25. Mai 2020 - 28. Mai 2020)

In: IEEE (ed.): **Proceedings of the 2020 IEEE Wireless Communications and Networking Conference (WCNC) 2020**

DOI: [10.1109/WCNC45663.2020.9120789](https://doi.org/10.1109/WCNC45663.2020.9120789)

BibTeX: [Download](#)

- Echavarria Gutiérrez JA., Wildermann S., Keszöcze O., Teich J.:

[Probabilistic Error Propagation through Approximated Boolean Networks](#)

57th Annual Design Automation Conference (DAC) (San Francisco, CA, 19. Juli 2020 - 23. Juli 2020)

In: **Proceedings of the 57th Annual Design Automation Conference 2020**

DOI: [10.1109/dac18072.2020.9218536](https://doi.org/10.1109/dac18072.2020.9218536)

BibTeX: [Download](#)

- Echavarria Gutiérrez JA., Wildermann S., Khosravi F., Teich J.:

[An Approximate Sequential Multiplier with Segmented Carry Chain and Variable Accuracy](#)

AxC20: 5th Workshop on Approximate Computing (San Francisco, CA, 19. Juli 2020 - 24. Juli 2020)

BibTeX: [Download](#)

- Groth S., Grünewald D., Teich J., Hannig F.:
[**A Runtime System for Finite Element Methods in a Partitioned Global Address Space**](#)
ACM International Conference on Computing Frontiers 2020 (Catania, Sicily, Italy, 11. Mai 2020 - 13. Mai 2020)
In: **Proceedings of the 17th ACM International Conference on Computing Frontiers (CF) 2020**
DOI: [10.1145/3387902.3392628](https://doi.org/10.1145/3387902.3392628)
BibTeX: [Download](#)
- [Heidorn C.](#), Hannig F., Teich J.:
[**Design Space Exploration for Layer-parallel Execution of Convolutional Neural Networks on CGRAs**](#)
International Workshop on Software and Compilers for Embedded Systems (SCOPES) (St. Goar, 25. Mai 2020 - 26. Mai 2020)
In: **Proceedings of the 23rd International Workshop on Software and Compilers for Embedded Systems (SCOPES) 2020**
DOI: [10.1145/3378678.3391878](https://doi.org/10.1145/3378678.3391878)
BibTeX: [Download](#)
- Herkersdorf A., Engel M., Glaß M., Henkel J., Kleeberger VB., Kühn JM., Marwedel P., Mueller-Gritschneider D., Nassif SR., Rehman S., Rosenstiel W., Schlichtmann U., Shafique M., Teich J., Wehn N., Weis C.:
[**RAP Model - Enabling Cross-Layer Analysis and Optimization for System-on-Chip Resilience**](#)
In: Henkel, Jörg, Dutt, Nikil (ed.): **Dependable Embedded Systems**, 2020
ISBN: 978-3-030-52017-5
DOI: [10.1007/978-3-030-52017-5_1](https://doi.org/10.1007/978-3-030-52017-5_1)
BibTeX: [Download](#)
- Keszöcze O., König M., Brand M., Teich J.:
[**Error Analysis for Loop Programs using Anytime Instructions in Approximate Computing**](#)
Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (Stuttgart, 19. März 2020 - 20. März 2020)
BibTeX: [Download](#)

- Lengauer C., Apel S., Bolten M., Chiba S., Rude U., Teich J., Großlinger A., Hannig F., Köstler H., Claus L., Grebhahn A., Groth S., Kronawitter S., Kuckuk S., Ritlich H., Schmitt C., Schmitt J.:

[ExaStencils: Advanced multigrid solver generation](#)

In: Hans-Joachim Bungartz, Severin Reiz, Benjamin Uekermann, Philipp Neumann, Wolfgang E. Nagel (ed.): **Lecture notes in computational science and engineering**, Cham: Springer, 2020, p. 405-452 (Software for Exascale Computing SPPEXA 2016 – 2019, Vol.136)

ISBN: 978-3-030-47955-8

DOI: [10.1007/978-3-030-47956-5](https://doi.org/10.1007/978-3-030-47956-5)

URL: https://library.open.org/bitstream/handle/20.500.12657/41289/2020_Book_SoftwareForExascaleComputing-S.pdf?sequence=1#page=411

BibTeX: [Download](#)

- Lengauer C., Apel S., Bolten M., Chiba S., Rude U., Teich J., Großlinger A., Hannig F., Köstler H., Claus L., Grebhahn A., Groth S., Kronawitter S., Kuckuk S., Ritlich H., Schmitt C., Schmitt J.:

[ExaStencils – Advanced Multigrid Solver Generation](#)

In: Hans-Joachim Bungartz, Severin Reiz, Philipp Neumann, Benjamin Uekermann, Wolfgang Nagel (ed.): **Software for Exascale Computing – SPPEXA 2016-2019**, Springer, 2020, p. 405-452 (Lecture Notes in Computer Science and Engineering, Vol.136)

ISBN: 978-3-030-47955-8

DOI: [10.1007/978-3-030-47956-5_14](https://doi.org/10.1007/978-3-030-47956-5_14)

URL: https://www12.cs.fau.de/downloads/hannig/publications/ExaStencils_Advanced_Multigrid_Solver_Generation.pdf

BibTeX: [Download](#)

- Letras M., [Falk J.](#), Schwarzer T., Teich J.:

[Multi-objective Optimization of Mapping Dataflow Applications to MPSoCs Using a Hybrid Evaluation Combining Analytic Models and Measurements](#)

In: **ACM Transactions on Design Automation of Electronic Systems** 26 (2020), p. 1–33

ISSN: 1084-4309

DOI: [10.1145/3431814](https://doi.org/10.1145/3431814)

BibTeX: [Download](#)

- Mattauch S., Lohmann K., Hannig F., Lohmann D., Teich J.:
[**A Bibliometric Approach for Detecting the Gender Gap in Computer Science**](#)
In: **Communications of the ACM** 63 (2020), p. 39-45
ISSN: 0001-0782
DOI: [10.1145/3376901](https://doi.org/10.1145/3376901)
BibTeX: [Download](#)
- Pourmohseni B., Glaß M., Henkel J., Khdr H., Rapp M., Richthammer V., Schwarzer T., Smirnov F., Spieck J., Teich J., Weichslgartner A., Wildermann S.:
[**Hybrid Application Mapping for Composable Many-Core Systems: Overview and Future Perspective**](#)
In: **Journal of Low Power Electronics and Applications** 10 (2020), p. 1-37
ISSN: 2079-9268
DOI: [10.3390/jlpea10040038](https://doi.org/10.3390/jlpea10040038)
URL: <https://www.mdpi.com/892470>
BibTeX: [Download](#)
- Pourmohseni B., Smirnov F., Wildermann S., Teich J.:
[**Real-Time Task Migration for Dynamic Resource Management in Many-Core Systems**](#)
Workshop on Next Generation Real-Time Embedded Systems (NG-RES) (Bologna, 21. Januar 2020)
In: **Proceedings of the Workshop on Next Generation Real-Time Embedded Systems (NG-RES) 2020**
DOI: [10.4230/OASlcs.NG-RES.2020.5](https://doi.org/10.4230/OASlcs.NG-RES.2020.5)
URL: <https://drops.dagstuhl.de/opus/volltexte/2020/11781/>
BibTeX: [Download](#)
- Pourmohseni B., Teich J.:
[**System-Level Mapping, Analysis, and Management of Real-Time Applications in Many-Core Systems**](#)
PhD Forum at the Design, Automation, and Test in Europe (DATE) Conference and Exhibition (Grenoble, France, 9. März 2020 - 13. März 2020)

URL: <https://www12.cs.fau.de/downloads/pourmohseni/pub/phdForum-DATE20.pdf>

BibTeX: [Download](#)

- Qiao B., Reiche O., Teich J., Hannig F.:
[**Unveiling Kernel Concurrency in Multiresolution Filters on GPUs with an Image Processing DSL**](#)
13th Workshop on General Purpose Processing Using GPU (GPGPU) (San Diego, CA, USA, 23. Februar 2020 - 23. Februar 2020)
In: **Proceedings of the 13th Workshop on General Purpose Processing Using GPU (GPGPU) 2020**
DOI: [10.1145/3366428.3380773](https://doi.org/10.1145/3366428.3380773)
BibTeX: [Download](#)
- Qiao B., Reiche O., Özkan MA., Teich J., Hannig F.:
[**Efficient Parallel Reduction on GPUs with Hipacc**](#)
23rd International Workshop on Software and Compilers for Embedded Systems (SCOPES) (Sankt Goar, 25. Mai 2020 - 26. Mai 2020)
In: **Proceedings of the 23rd International Workshop on Software and Compilers for Embedded Systems (SCOPES) 2020**
DOI: [10.1145/3378678.3391885](https://doi.org/10.1145/3378678.3391885)
BibTeX: [Download](#)
- Qiao B., Özkan MA., Teich J., Hannig F.:
[**The Best of Both Worlds: Combining CUDA Graph with an Image Processing DSL**](#)
57th Annual Design Automation Conference (DAC) (San Francisco, CA, 19. Juli 2020 - 23. Juli 2020)
In: **Proceedings of the 57th Annual Design Automation Conference (DAC) 2020**
DOI: [10.1109/DAC18072.2020.9218531](https://doi.org/10.1109/DAC18072.2020.9218531)
BibTeX: [Download](#)
- Sabih M., Hannig F., Teich J.:
[**Utilizing Explainable AI for Quantization and Pruning of Deep Neural Networks**](#)
(2020)

Open Access: <https://arxiv.org/pdf/2008.09072>

URL: <https://arxiv.org/abs/2008.09072>

BibTeX: [Download](#)

(online publication)

- Simon B., [Falk J.](#), Megow N., Teich J.:

[Energy Minimization in DAG Scheduling on MPSoCs at Run-Time: Theory and Practice](#)

Workshop on Next Generation Real-Time Embedded Systems (Bologna, 21. Januar 2020)

In: **Proceedings of the Workshop on Next Generation Real-Time Embedded Systems (NG-RES) 2020**

DOI: [10.4230/OASlcs.NG-RES.2020.2](https://doi.org/10.4230/OASlcs.NG-RES.2020.2)

URL: <https://drops.dagstuhl.de/opus/volltexte/2020/11778/>

BibTeX: [Download](#)

- Smirnov F., Pourmohseni B., Teich J.:

[Using Learning Classifier Systems for the DSE of Adaptive Embedded Systems](#)

Design, Automation and Test in Europe Conference and Exhibition (DATE) (Grenoble)

In: **PROCEEDINGS OF THE 2020 DESIGN, AUTOMATION & TEST IN EUROPE CONFERENCE & EXHIBITION (DATE 2020)**, NEW YORK: 2020

DOI: [10.23919/date48585.2020.9116383](https://doi.org/10.23919/date48585.2020.9116383)

BibTeX: [Download](#)

- Smirnov F., Pourmohseni B., Teich J.:

[Using Learning Classifier Systems for the DSE of Dynamically Adaptable Embedded Systems](#)

Design, Automation and Test in Europe Conference (Grenoble, 9. März 2020 - 13. März 2020)

BibTeX: [Download](#)

- Spieck J., Wildermann S., Teich J.:

[Run-Time Scenario-Based MPSoC Mapping Reconfiguration Using Machine Learning Models](#)

1st ACM/IEEE Workshop on Machine Learning for CAD (MLCAD) (Canmore, Alberta, Canada, 3. September 2019 - 4. September 2019)

In: **Post-workshop proceedings of 2019 ACM/IEEE 1st Workshop on Machine Learning for CAD 2020**

DOI: [10.1109/MLCAD48534.2019.9142060](https://doi.org/10.1109/MLCAD48534.2019.9142060)

BibTeX: [Download](#)

- Spieck J., Wildermann S., Teich J.:
[Scenario-Based Soft Real-Time Hybrid Application Mapping for MPSoCs](#)
57th Annual Design Automation Conference (DAC) (San Francisco, 19. Juli 2020 - 23. Juli 2020)
In: **Proceedings of the 57th Annual Design Automation Conference (DAC) 2020**
DOI: [10.1109/DAC18072.2020.9218537](https://doi.org/10.1109/DAC18072.2020.9218537)
BibTeX: [Download](#)
- Streit FJ., Fritz F., Becher A., Wildermann S., Werner S., Schmidt-Korth M., Pschyklenk M., Teich J.:
[Secure Boot from Non-Volatile Memory for Programmable SoC-Architectures](#)
International Symposium on Hardware Oriented Security and Trust (HOST) (San José, USA, 7. Dezember 2020 - 11. Dezember 2020)
In: **IEEE Proceedings of the 13th International Symposium on Hardware Oriented Security and Trust 2020**
DOI: [10.1109/HOST45689.2020.9300126](https://doi.org/10.1109/HOST45689.2020.9300126)
BibTeX: [Download](#)
- Streit FJ., Wituschek S., Pschyklenk M., Becher A., Lechner M., Wildermann S., Pitz I., Merklein M., Teich J.:
[Data acquisition and control at the edge: a hardware/software-reconfigurable approach](#)
In: **Production Engineering** 14 (2020), p. 365-371
ISSN: 0944-6524
DOI: [10.1007/s11740-020-00964-x](https://doi.org/10.1007/s11740-020-00964-x)
BibTeX: [Download](#)

- Teich J., Mahmoody P., Pourmohseni B., Roloff S., Schröder-Preikschat W., Wildermann S.:
[Run-Time Enforcement of Non-functional Program Properties on MPSoCs](#)
In: Jian-Jia Chen (ed.): **A Journey of Embedded and Cyber-Physical Systems**, Springer, 2020
ISBN: 978-3-030-47487-4
DOI: [10.1007/978-3-030-47487-4](https://doi.org/10.1007/978-3-030-47487-4)
BibTeX: [Download](#)
- Teich J., Pourmohseni B., Keszöcze O., Spieck J., Wildermann S.:
[Run-Time Enforcement of Non-Functional Application Requirements in Heterogeneous Many-Core Systems](#)
Asia and South Pacific Design Automation Conference (ASP-DAC) (China National Convention Center, Beijing, China, 13. Januar 2020 - 16. Januar 2020)
DOI: [10.1109/ASP-DAC47756.2020.9045536](https://doi.org/10.1109/ASP-DAC47756.2020.9045536)
BibTeX: [Download](#)
- Traiola M., Echavarria Gutiérrez JA., Bosio A., Teich J., O'Connor I.:
[Design Space Exploration of an Approximation-Based Fully Reliable TMR Alternative](#)
8th Prague Embedded Systems Workshop (Horoměřice, 6. November 2020 - 7. November 2020)
Open Access: https://www12.cs.fau.de/downloads/echavarria/pub/Design_Space_Exploration_of_an_Approximation-Based_Fully_Reliable_TMR_Alternative.pdf
BibTeX: [Download](#)
- Walter D., Witterauf M., Teich J.:
[Real-time Scheduling of I/O Transfers for Massively Parallel Processor Arrays](#)
18th ACM-IEEE International Conference on Formal Methods and Models for System Design, MEMOCODE 2020 (Jaipur, India, 2. Dezember 2020 - 4. Dezember 2020)
In: **Proceedings of the 18th ACM-IEEE International Conference on Formal Methods and Models for System Design (MEMOCODE) 2020**

DOI: [10.1109/MEMOCODE51338.2020.9315179](https://doi.org/10.1109/MEMOCODE51338.2020.9315179)

BibTeX: [Download](#)

- Wang B., Glaß M., [Falk J.](#), Ahmed I., Teich J.:

[**Exploration of Power Domain Partitioning with Concurrent Task Mapping and Scheduling for Application-specific Multi-core SoCs**](#)

33rd International Conference on Architecture of Computing Systems (ARCS) (Aachen, 25. Mai 2020 - 28. Mai 2020)

In: **In Proc. of the 33rd International Conference on Architecture of Computing Systems (ARCS) 2020**

DOI: [10.1007/978-3-030-52794-5_12](https://doi.org/10.1007/978-3-030-52794-5_12)

BibTeX: [Download](#)

- Özkan MA., Pérard-Gayot A., Membarth R., Slusallek P., Leißen R., Hack S., Teich J., Hannig F.:

[**AnyHLS: High-Level Synthesis with Partial Evaluation**](#)

International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) (Hamburg, 20. September 2020 - 25. September 2020)

DOI: [10.1109/tcad.2020.3012172](https://doi.org/10.1109/tcad.2020.3012172)

URL: <https://arxiv.org/pdf/2002.05796.pdf>

BibTeX: [Download](#)

- Özkan MA., Pérard-Gayot A., Membarth R., Slusallek P., Leißen R., Hack S., Teich J., Hannig F.:

[**AnyHLS: High-Level Synthesis with Partial Evaluation**](#)

In: **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems** 39 (2020), p. 3202-3214

ISSN: 0278-0070

DOI: [10.1109/TCAD.2020.3012172](https://doi.org/10.1109/TCAD.2020.3012172)

URL: <https://arxiv.org/pdf/2002.05796.pdf>

BibTeX: [Download](#)

2019

- Ah Sue J., Brand P., [Falk J.](#), Hasholzner R., Teich J.:

[**Optimizing Exploratory Workflows for Embedded Platform Trace Analysis and its Application to Cellular Modems**](#)

21st Int. Conf. on Human-Computer Interaction (Orlando, Florida, USA, 26. Juli 2019 - 31. Juli 2019)

In: **HCII 2019 Late Breaking Work Papers Proceedings**, New York, NY, USA: 2019

DOI: [10.1007/978-3-030-30033-3_10](https://doi.org/10.1007/978-3-030-30033-3_10)

BibTeX: [Download](#)

- Aliee H., Khosravi F., Teich J.:

[Efficient Treatment of Uncertainty in System Reliability Analysis using Importance Measures](#)

Dependable Systems and Networks (DSN) (Portland, Oregon, USA, 24. Juni 2019 - 27. Juni 2019)

In: **The 49th IEEE/IFIP International Conference on Dependable Systems and Networks 2019**

DOI: [10.1109/dsn.2019.00022](https://doi.org/10.1109/dsn.2019.00022)

BibTeX: [Download](#)

- Becher A., Herrmann A., Wildermann S., Teich J.:

[ReProVide: Towards Utilizing Heterogeneous Partially Reconfigurable Architectures for Near-Memory Data Processing](#)

1st Workshop on Novel Data Management Ideas on Heterogeneous (Co-)Processors (NoDMC) at 18. Fachtagung für "Datenbanksysteme für Business, Technologie und Web" (Universität Rostock, 4. März 2019 - 8. März 2019)

In: Gesellschaft für Informatik, Bonn (ed.): **Proceedings of the 1st Workshop on Novel Data Management Ideas on Heterogeneous (Co-)Processors (NoDMC)**, Bonn: 2019

DOI: [10.18420/btw2019-ws-04](https://doi.org/10.18420/btw2019-ws-04)

URL: <https://dl.gi.de/handle/20.500.12116/21825>

BibTeX: [Download](#)

- Becher A., Teich J.:

[In situ Statistics Generation within partially reconfigurable Hardware Accelerators for Query Processing](#)

15th International Workshop on Data Management on New Hardware (DaMoN) Held with ACM SIGMOD/PODS 2019 (Amsterdam, 1. Juli 2019 - 1. Juli 2019)

DOI: [10.1145/3329785.3329936](https://doi.org/10.1145/3329785.3329936)

BibTeX: [Download](#)

- Brand M., Witterauf M., Hannig F., Teich J.:

[Anytime Instructions for Programmable Accuracy Floating-Point Arithmetic](#)

ACM International Conference on Computing Frontiers 2019 (Alghero, Sardinia, 30. April 2019 - 2. Mai 2019)

DOI: [10.1145/3310273.3322833](https://doi.org/10.1145/3310273.3322833)

BibTeX: [Download](#)

- Brand M., Witterauf M., Sousa É., Tanase AP., Hannig F., Teich J.:

[*-Predictable MPSoC Execution of Real-Time Control Applications Using Invasive Computing](#)

In: **Concurrency and Computation-Practice & Experience** (2019)

ISSN: 1532-0626

DOI: [10.1002/cpe.5149](https://doi.org/10.1002/cpe.5149)

BibTeX: [Download](#)

- Fickenscher J., Hannig F., Teich J.:

[DSL-based Acceleration of Automotive Environment Perception and Mapping Algorithms for embedded CPUs, GPUs, and FPGAs](#)

ARCS 2019 - 32nd International Conference on Architecture of Computing Systems (Copenhagen, 20. Mai 2019 - 23. Mai 2019)

In: Martin Schoeberl, Christian Hochberger, Sascha Uhrig, Jürgen Brehm, Thilo Pionteck (ed.): **Proceedings of the 32nd International Conference on Architecture of Computing Systems (ARCS) 2019**

DOI: [10.1007/978-3-030-18656-2](https://doi.org/10.1007/978-3-030-18656-2)

BibTeX: [Download](#)

- Groth S., Schmitt C., Teich J., Hannig F.:

[SYCL Code Generation for Multigrid Methods](#)

22nd International Workshop on Software and Compilers for Embedded Systems (SCOPES '19) (Sankt Goar, Germany, 27. Mai 2019 - 29. Mai 2019)

In: **22nd International Workshop on Software and Compilers for Embedded Systems (SCOPES '19) 2019**

DOI: [10.1145/3323439.3323984](https://doi.org/10.1145/3323439.3323984)

BibTeX: [Download](#)

- [Heidorn C.](#), Witterauf M., Hannig F., Teich J.:
[**Efficient Mapping of CNNs onto Tightly Coupled Processor Arrays**](#)
In: **Journal of Computers** 14 (2019), p. 541-556
ISSN: 1796-203X
DOI: [10.17706/jcp.14.8.541-556](https://doi.org/10.17706/jcp.14.8.541-556)
BibTeX: [Download](#)
- Letras M., [Falk J.](#), Schwarzer T., Teich J.:
[**On the Analytic Evaluation of Schedules via Max-Plus Algebra for DSE of Multi-Core Architectures**](#)
22nd International Workshop on Software and Compilers for Embedded Systems, (SCOPES) (Sankt Goar, Germany, 27. Mai 2019 - 28. Mai 2019)
In: **Proceedings of the 22st International Workshop on Software and Compilers for Embedded Systems, SCOPES 2019, Sankt Goar, Germany 2019**
DOI: [10.1145/3323439.3323979](https://doi.org/10.1145/3323439.3323979)
BibTeX: [Download](#)
- Membarth R., Dutta H., Hannig F., Teich J.:
[**Efficient Mapping of Streaming Applications for Image Processing on Graphics Cards**](#)
In: **Transactions on High-Performance Embedded Architectures and Compilers V**, Springer, 2019, p. 1-20 (Lecture Notes in Computer Science (LNCS), Vol.11225)
ISBN: 978-3-662-58833-8
DOI: [10.1007/978-3-662-58834-5_1](https://doi.org/10.1007/978-3-662-58834-5_1)
BibTeX: [Download](#)
- Nisar A., Ah Sue J., Teich J.:
[**Performance Comparison between Machine Learning based LTE Downlink Grant Predictors**](#)
21st International Conference on Artificial Intelligence (Las Vegas, 29. Juli 2019 - 1. August 2019)
In: **Proceedings of the 21st International Conference on Artificial Intelligence 2019**
BibTeX: [Download](#)

- [Plagwitz P.](#), Streit F.J., Becher A., Wildermann S., Teich J.:
Compiler-Based High-Level Synthesis of Application-Specific Processors on FPGAs
International Conference on ReConFigurable Computing and FPGAs (ReConFig) (Cancún, Mexico, 9. Dezember 2019 - 11. Dezember 2019)
In: **IEEE Proceedings of the 14th International Conference on ReConFigurable Computing and FPGAs 2019**
DOI: [10.1109/ReConFig48160.2019.8994778](https://doi.org/10.1109/ReConFig48160.2019.8994778)
BibTeX: [Download](#)
- Pourmohseni B., Smirnov F., Khdr H., Wildermann S., Teich J., Henkel J.:
Thermally Composable Hybrid Application Mapping for Real-Time Applications in Heterogeneous Many-Core Systems
IEEE Real-Time Systems Symposium (RTSS) (Hong Kong, 3. Dezember 2019 - 6. Dezember 2019)
In: **Proceedings of the 40th IEEE Real-Time Systems Symposium (RTSS) 2019**
DOI: [10.1109/RTSS46320.2019.00029](https://doi.org/10.1109/RTSS46320.2019.00029)
BibTeX: [Download](#)
- Pourmohseni B., Smirnov F., Wildermann S., Teich J.:
Isolation-Aware Timing Analysis and Design Space Exploration for Predictable and Composable Many-Core Systems
Euromicro Conference on Real-Time Systems (ECRTS) (Stuttgart, Germany, 9. Juli 2019 - 12. Juli 2019)
In: **Proceedings of the 31th Euromicro Conference on Real-Time Systems (ECRTS) 2019**
DOI: [10.4230/LIPIcs.ECRTS.2019.12](https://doi.org/10.4230/LIPIcs.ECRTS.2019.12)
URL: <http://drops.dagstuhl.de/opus/volltexte/2019/10749>
BibTeX: [Download](#)
- Pourmohseni B., Wildermann S., Glaß M., Teich J.:
Hard Real-Time Application Mapping Reconfiguration for NoC-Based Many-Core Systems
In: **Real-Time Systems** (2019), p. 1-37
ISSN: 0922-6443

DOI: [10.1007/s11241-019-09326-y](https://doi.org/10.1007/s11241-019-09326-y)

URL: <http://link.springer.com/article/10.1007/s11241-019-09326-y>

BibTeX: [Download](#)

- Qiao B., Reiche O., Hannig F., Teich J.:

[From Loop Fusion to Kernel Fusion: A Domain-specific Approach to Locality Optimization](#)

2019 International Symposium on Code Generation and Optimization (CGO) (Washington, DC, USA, 16. Februar 2019 - 20. Februar 2019)

In: **Proceedings of the 2019 IEEE/ACM International Symposium on Code Generation and Optimization (CGO) 2019**

DOI: [10.1109/CGO.2019.8661176](https://doi.org/10.1109/CGO.2019.8661176)

BibTeX: [Download](#)

- Roloff S., Hannig F., Teich J.:

[ActorX10 and Run-Time Application Embedding](#)

In: Sascha Roloff, Frank Hannig, Jürgen Teich (ed.): **Modeling and Simulation of Invasive Applications and Architectures**, 2019, p. 129-164 (Computer Architecture and Design Methodologies)

DOI: [10.1007/978-981-13-8387-8_6](https://doi.org/10.1007/978-981-13-8387-8_6)

BibTeX: [Download](#)

- Roloff S., Hannig F., Teich J.:

[Fundamentals](#)

In: Sascha Roloff, Frank Hannig, Jürgen Teich (ed.): **Modeling and Simulation of Invasive Applications and Architectures**, 2019, p. 9-40 (Computer Architecture and Design Methodologies)

DOI: [10.1007/978-981-13-8387-8_2](https://doi.org/10.1007/978-981-13-8387-8_2)

BibTeX: [Download](#)

- Roloff S., Hannig F., Teich J.:

[Hybrid Network-on-Chip Simulation](#)

In: Sascha Roloff, Frank Hannig, Jürgen Teich (ed.): **Modeling and Simulation of Invasive Applications and Architectures**, 2019, p. 77-99 (Computer Architecture and Design Methodologies)

DOI: [10.1007/978-981-13-8387-8_4](https://doi.org/10.1007/978-981-13-8387-8_4)

BibTeX: [Download](#)

- Roloff S., Hannig F., Teich J.:
[Introduction](#)
In: Sascha Roloff, Frank Hannig, Jürgen Teich (ed.): **Modeling and Simulation of Invasive Applications and Architectures**, 2019, p. 1-7 (Computer Architecture and Design Methodologies)
DOI: [10.1007/978-981-13-8387-8_1](https://doi.org/10.1007/978-981-13-8387-8_1)
BibTeX: [Download](#)
- Roloff S., Hannig F., Teich J.:
[InvadeSIM-A Simulation Framework for Invasive Parallel Programs and Architectures](#)
In: Sascha Roloff, Frank Hannig, Jürgen Teich (ed.): **Modeling and Simulation of Invasive Applications and Architectures**, 2019, p. 41-76 (Computer Architecture and Design Methodologies)
DOI: [10.1007/978-981-13-8387-8_3](https://doi.org/10.1007/978-981-13-8387-8_3)
BibTeX: [Download](#)
- Roloff S., Hannig F., Teich J.:
[Modeling and Simulation of Invasive Applications and Architectures](#)
Singapore: Springer, 2019
(Computer Architecture and Design Methodologies)
ISBN: 978-981-13-8386-1
DOI: [10.1007/978-981-13-8387-8](https://doi.org/10.1007/978-981-13-8387-8)
BibTeX: [Download](#)
- Roloff S., Hannig F., Teich J.:
[Modeling and Simulation of Invasive Applications and Architectures Conclusions and Future Directions](#)
In: Sascha Roloff, Frank Hannig, Jürgen Teich (ed.): **Modeling and Simulation of Invasive Applications and Architectures**, 2019, p. 165-168 (Computer Architecture and Design Methodologies)
DOI: [10.1007/978-981-13-8387-8_7](https://doi.org/10.1007/978-981-13-8387-8_7)
BibTeX: [Download](#)
- Roloff S., Hannig F., Teich J.:
[Parallel MPSoC Simulation and Architecture Evaluation](#)
In: Sascha Roloff, Frank Hannig, Jürgen Teich (ed.): **Modeling and Simulation**

of Invasive Applications and Architectures, 2019, p. 101-128 (Computer Architecture and Design Methodologies)

DOI: [10.1007/978-981-13-8387-8_5](https://doi.org/10.1007/978-981-13-8387-8_5)

BibTeX: [Download](#)

- Schwarzer T., [Falk J.](#), Müller S., Letras M., [Heidorn C.](#), Wildermann S., Teich J.:
[**Compilation of Dataflow Applications for Multi-Cores using Adaptive Multi-Objective Optimization**](#)

In: **ACM Transactions on Design Automation of Electronic Systems** 24 (2019), Article No.: 29

ISSN: 1084-4309

DOI: [10.1145/3310249](https://doi.org/10.1145/3310249)

BibTeX: [Download](#)

- Smirnov F., Pourmohseni B., GLAß M., Teich J.:
[**Igor, get me the optimum! Prioritizing important design decisions during the DSE of embedded systems**](#)

In: **Transactions on Embedded Computing Systems** 18 (2019), Article No.: a78

ISSN: 1558-3465

DOI: [10.1145/3358204](https://doi.org/10.1145/3358204)

BibTeX: [Download](#)

- Smirnov F., Pourmohseni B., Glaß M., Teich J.:
[**IGOR, get me the Optimum! Prioritizing Important Design Decisions During the DSE of Embedded Systems**](#)

CODES+ISSS: International Conference on Hardware/Software Codesign and System Synthesis (New York, NY, 13. Oktober 2019 - 18. Oktober 2019)

DOI: [10.1145/3358204](https://doi.org/10.1145/3358204)

BibTeX: [Download](#)

- Smirnov F., Pourmohseni B., Glaß M., Teich J.:
[**Variety-Aware Routing Encoding for Efficient Design Space Exploration of Automotive Communication Networks**](#)

5th International Conference on Vehicle Technology and Intelligent Transport Systems (VEHITS) (Heraklion, Kreta, 3. Mai 2019 - 5. Mai 2019)

BibTeX: [Download](#)

- Spieck J., Wildermann S., Schwarzer T., Teich J., Glaß M.:
[Data-Driven Scenario-based Application Mapping for Heterogeneous Many-Core Systems](#)
IEEE Multicore/Many-core Systems-on-Chip (Singapore, 1. Oktober 2019 - 4. Oktober 2019)
In: **Multicore/Many-core Systems-on-Chip (MCSoc 2019)** 2019
DOI: [10.1109/MCSoc.2019.00054](https://doi.org/10.1109/MCSoc.2019.00054)
BibTeX: [Download](#)
- Teich J., Fummi F.:
[Conference Reports: Recap of DATE 2019 in Florence, Italy](#)
In: **IEEE Design & Test** 36 (2019), p. 59-61
ISSN: 2168-2356
DOI: [10.1109/MDAT.2019.2915112](https://doi.org/10.1109/MDAT.2019.2915112)
BibTeX: [Download](#)
- Teich J., Fummi F.:
[Design, Automation & Test in Europe Conference & Exhibition, DATE 2019, Florence, Italy, March 25-29, 2019](#)
2019
ISBN: 978-3-9819263-2-3
DOI: [10.1109/MDAT.2019.2915112](https://doi.org/10.1109/MDAT.2019.2915112)
BibTeX: [Download](#)
- Witterauf M., Hannig F., Teich J.:
[Polyhedral Fragments: An Efficient Representation for Symbolically Generating Code for Processor Arrays](#)
International Conference on Formal Methods and Models for System Design (MEMOCODE) (San Diego, 9. Oktober 2019 - 11. Oktober 2019)
In: **Proceedings of the International Conference on Formal Methods and Models for System Design (MEMOCODE)** 2019
BibTeX: [Download](#)
- Özkan MA., Reiche O., Qiao B., Membarth R., Teich J., Hannig F.:
[Synthesizing High-Performance Image Processing Applications with Hipacc](#)
Demo at the University Booth at Design, Automation and Test in Europe (DATE) (Florence, 25. März 2019 - 29. März 2019)

URL: <https://www12.cs.fau.de/downloads/oezkan/publications/date-ubooth19.pdf>

BibTeX: [Download](#)

(online publication)

2018

- Afzal A., Schmitt C., Alhaddad S., Grynko Y., Teich J., Förstner J., Hannig F.:
[Solving Maxwell's Equations with Modern C++ and SYCL: A Case Study](#)
The 29th Annual IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP) (Politecnico di Milano, Milan, 10. Juli 2018 - 12. Juli 2018)
In: **Proceedings of the 29th Annual IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP) 2018**
DOI: [10.1109/ASAP.2018.8445127](https://doi.org/10.1109/ASAP.2018.8445127)
URL: <https://www12.cs.fau.de/downloads/schmittch/publications/A-SAGTFH18asap.pdf>
BibTeX: [Download](#)
- Ah Sue J., Brand P., Brendel J., Hasholzner R., [Falk J.](#), Teich J.:
[A Predictive Dynamic Power Management for LTE-Advanced Mobile Devices](#)
IEEE Wireless Communications and Networking Conference (Barcelona, Catalonia, Spain, 15. April 2018 - 18. April 2018)
In: IEEE (ed.): **2018 IEEE Wireless Communications and Networking Conference (WCNC'18) 2018**
DOI: [10.1109/WCNC.2018.8377189](https://doi.org/10.1109/WCNC.2018.8377189)
BibTeX: [Download](#)
- Becher A., Beena Gopalakrishnan Nair L., Broneske D., Drewes T., Gurumurthy B., Meyer-Wegener K., Pionteck T., Saake G., Teich J., Wildermann S.:
[Integration of FPGAs in Database Management Systems: Challenges and Opportunities](#)
In: **Datenbank-Spektrum (2018)**
ISSN: 1618-2162
DOI: [10.1007/s13222-018-0294-9](https://doi.org/10.1007/s13222-018-0294-9)
BibTeX: [Download](#)

- Becher A., Wildermann S., Teich J.:
[Optimistic Regular Expression Matching on FPGAs for Near-Data Processing](#)
Data Management on New Hardware (DaMoN) (Houston, Texas, 11. Juni 2018 - 11. Juni 2018)
DOI: [10.1145/3211922.3211926](https://doi.org/10.1145/3211922.3211926)
BibTeX: [Download](#)
- Brand P., [Falk J.](#), Ah Sue J., Brendel J., Hasholzner R., Teich J.:
[Reinforcement Learning for Power-Efficient Grant Prediction in LTE](#)
(2018), p. 18-26
DOI: [10.1145/3207719.3207722](https://doi.org/10.1145/3207719.3207722)
BibTeX: [Download](#)
- Echavarria Gutiérrez JA., Schütz K., Becher A., Wildermann S., Teich J.:
[Can Approximate Computing Reduce Power Consumption on FPGAs?](#)
25th IEEE International Conference on Electronics Circuits and Systems (Bordeaux, 9. Dezember 2018 - 12. Dezember 2018)
In: **Proceedings of IEEE International Conference on Electronics Circuits and Systems 2018**
DOI: [10.1109/icecs.2018.8618062](https://doi.org/10.1109/icecs.2018.8618062)
BibTeX: [Download](#)
- Echavarria Gutiérrez JA., Schütz K., Becher A., Wildermann S., Teich J.:
[Evaluation of Approximate Computing Techniques for Power Reduction on FPGAs](#)
AxC18: 3rd Workshop on Approximate Computing (Swissôtel Bremen, 31. Mai 2018 - 1. Juni 2018)
Open Access: https://www12.cs.fau.de/downloads/echavarria/pub/Evaluation_of_Approximate_Computing_Techniques_for_Power_Reduction_on_FPGAs.pdf
BibTeX: [Download](#)
- Echavarria Gutiérrez JA., Wildermann S., Teich J.:
[AConFPGA: A Multiple-Output Boolean Function Approximation DSE Technique Targeting FPGAs](#)
International Conference on Field Programmable Technology (FPT 2018) (Naha,

Okinawa, 10. Dezember 2018 - 14. Dezember 2018)

In: **Proceedings of 2018 International Conference on Field Programmable Technology 2018**

DOI: [10.1109/fpt.2018.00065](https://doi.org/10.1109/fpt.2018.00065)

BibTeX: [Download](#)

- Echavarria Gutiérrez JA., Wildermann S., Teich J.:
[Design Space Exploration of Multi-output Logic Function Approximations](#)
International Conference On Computer Aided Design (ICCAD 2018) (San Diego, CA, 5. November 2018 - 8. November 2018)
In: **Proceedings of the International Conference On Computer Aided Design 2018**
DOI: [10.1145/3240765.3240795](https://doi.org/10.1145/3240765.3240795)
BibTeX: [Download](#)
- [Falk J.](#), Neubauer K., Haubelt C., Zebelein C., Teich J.:
[Integrated Modeling Using Finite State Machines and Dataflow Graphs](#)
In: Bhattacharyya S., Deprettere E., Leupers R., Takala J. (ed.): **Handbook of Signal Processing Systems**, Springer, 2018, p. 825-864
ISBN: 978-3-319-91734-4
DOI: [10.1007/978-3-319-91734-4_23](https://doi.org/10.1007/978-3-319-91734-4_23)
BibTeX: [Download](#)
- Fickenscher J., Hannig F., Bouzouraa ME., Teich J.:
[Embedded GPUs in Future Automated Cars](#)
Design, Automation and Test in Europe (DATE) (Dresden, 19. März 2018 - 23. März 2018)
BibTeX: [Download](#)
(Working Paper)
- Fickenscher J., Hannig F., Teich J., Bouzouraa ME.:
[Base Algorithms of Environment Maps and Efficient Occupancy Grid Mapping on Embedded GPUs](#)
4th International Conference on Vehicle Technology and Intelligent Transport Systems (VEHITS) (Funchal, Madeira, Portugal, 16. März 2018 - 18. März 2018)
DOI: [10.5220/0006677302980306](https://doi.org/10.5220/0006677302980306)
BibTeX: [Download](#)

- Fickenscher J., Schlumberger J., Hannig F., Bouzouraa ME., Teich J.:
[Cell-based Update Algorithm for Occupancy Grid Maps and new Hybrid Map for ADAS on Embedded GPUs](#)
Design, Automation and Test in Europe (DATE) (Dresden, Germany, 19. März 2018 - 23. März 2018)
DOI: [10.23919/DATE.2018.8342050](https://doi.org/10.23919/DATE.2018.8342050)
BibTeX: [Download](#)
- Fickenscher J., Schmidt S., Hannig F., Bouzouraa ME., Teich J.:
[Path Planning for Highly Automated Driving on Embedded GPUs](#)
4 (2018)
ISSN: 2079-9268
DOI: [10.3390/jlpea8040035](https://doi.org/10.3390/jlpea8040035)
BibTeX: [Download](#)
- Henkel J., Teich J., Wildermann S., Amrouch H.:
[Dynamic Resource Management for Heterogeneous Many-Cores](#)
International Conference On Computer Aided Design (ICCAD 2018) (San Diego, CA, 5. November 0018 - 8. November 0018)
In: **Proceedings of International Conference On Computer Aided Design 2018** 2018
DOI: [10.1145/3240765.3243471](https://doi.org/10.1145/3240765.3243471)
BibTeX: [Download](#)
- Khosravi F., Borst M., Teich J.:
[Probabilistic Dominance in Robust Multi-Objective Optimization](#)
IEEE Congress on Evolutionary Computation (CEC) (Barra da Tijuca, Rio de Janeiro, 8. Juli 2018 - 13. Juli 2018)
In: **IEEE Congress on Evolutionary Computation (CEC) 2018**
DOI: [10.1109/CEC.2018.8477676](https://doi.org/10.1109/CEC.2018.8477676)
URL: <https://ieeexplore.ieee.org/abstract/document/8477676>
BibTeX: [Download](#)
- Khosravi F., Müller M., Glaß M., Teich J.:
[Simulation-based Uncertainty Correlation Modeling in Reliability Analysis](#)
In: **Proceedings of the Institution of Mechanical Engineers, Part O: Journal of Risk and Reliability** 232 (2018), p. 725-737

ISSN: 1748-006X

DOI: [10.1177/1748006X18758720](https://doi.org/10.1177/1748006X18758720)

URL: <https://journals.sagepub.com/doi/abs/10.1177/1748006X18758720>

BibTeX: [Download](#)

- Mattauch S., Lohmann K., Hannig F., Lohmann D., Teich J.:
[The Gender Gap in Computer Science --- A Bibliometric Analysis](#)
(2018)
ISSN: 2191-5008
DOI: [10.25593/issn.2191-5008/CS-2018-02](https://doi.org/10.25593/issn.2191-5008/CS-2018-02)
BibTeX: [Download](#)
(Techreport)
- Mitra T., Teich J., Thiele L.:
[Guest Editors' Introduction: Special Issue on Time-Critical Systems Design](#)
In: **IEEE Design and Test of Computers** 35 (2018), p. 5-7
ISSN: 0740-7475
DOI: [10.1109/MDAT.2018.2796037](https://doi.org/10.1109/MDAT.2018.2796037)
BibTeX: [Download](#)
- Mitra T., Teich J., Thiele L.:
[Guest Editors' Introduction: Special Issue on Time-Critical Systems Design Part II](#)
In: **IEEE Design and Test of Computers** 35 (2018), p. 5 - 6
ISSN: 0740-7475
DOI: [10.1109/MDAT.2018.2841769](https://doi.org/10.1109/MDAT.2018.2841769)
BibTeX: [Download](#)
- Mitra T., Teich J., Thiele L.:
[Time-Critical Systems Design: A Survey](#)
In: **IEEE Design and Test of Computers** 35 (2018), p. 8-26
ISSN: 0740-7475
DOI: [10.1109/MDAT.2018.2794204](https://doi.org/10.1109/MDAT.2018.2794204)
BibTeX: [Download](#)
- Qiao B., Reiche O., Hannig F., Teich J.:
[Automatic Kernel Fusion for Image Processing DSLs](#)
21st International Workshop on Software and Compilers for Embedded Systems

(SCOPES) (Sankt Goar, 28. Mai 2018 - 30. Mai 2018)

In: **Proceedings of the 21th International Workshop on Software and Compilers for Embedded Systems (SCOPES) 2018**

DOI: [10.1145/3207719.3207723](https://doi.org/10.1145/3207719.3207723)

BibTeX: [Download](#)

- Reiche O., Özkan MA., Hannig F., Teich J., Schmid M.:

[Loop Parallelization Techniques for FPGA Accelerator Synthesis](#)

In: **Journal of Signal Processing Systems** 90 (2018), p. 3-27

ISSN: 1939-8115

DOI: [10.1007/s11265-017-1229-7](https://doi.org/10.1007/s11265-017-1229-7)

BibTeX: [Download](#)

- Richthammer V., Schwarzer T., Wildermann S., Teich J., Glaß M.:

[Architecture Decomposition in System Synthesis of Heterogeneous Many-Core Systems](#)

55th ACM/EDAC/IEEE Design Automation Conference (DAC 2018) (San Francisco, CA, 24. Juni 2018 - 28. Juni 2018)

DOI: [10.1109/DAC.2018.8465811](https://doi.org/10.1109/DAC.2018.8465811)

BibTeX: [Download](#)

- Schmitt C., Hannig F., Teich J.:

[A Target Platform Description Language for Parallel Code Generation](#)

31st GI/ITG International Conference on Architecture of Computing Systems (ARCS) (Braunschweig, 9. April 2018 - 12. April 2018)

In: **Workshop Proceedings of the 31st GI/ITG International Conference on Architecture of Computing Systems (ARCS)**, Berlin: 2018

URL: <https://www12.cs.fau.de/downloads/schmittch/publications/SHT18arcs.pdf>

BibTeX: [Download](#)

- Schmitt C., Kronawitter S., Hannig F., Teich J., Lengauer C.:

[Automating the Development of High-Performance Multigrid Solvers](#)

In: **Proceedings of the IEEE** 106 (2018), p. 1969-1984

ISSN: 0018-9219

DOI: [10.1109/JPROC.2018.2854229](https://doi.org/10.1109/JPROC.2018.2854229)

BibTeX: [Download](#)

- Schmitt C., Schmid M., Kuckuk S., Köstler H., Teich J., Hannig F.:
[Reconfigurable Hardware Generation of Multigrid Solvers with Conjugate Gradient Coarse-Grid Solution](#)
In: **Parallel Processing Letters** 28 (2018), Article No.: 1850016
ISSN: 0129-6264
DOI: [10.1142/S0129626418500160](https://doi.org/10.1142/S0129626418500160)
BibTeX: [Download](#)
- Schwarzer T., Roloff S., Richthammer V., Khaldi R., Wildermann S., Glaß M., Teich J.:
[On the Complexity of Mapping Feasibility in Many-Core Architectures](#)
Multicore/Many-core Systems-on-Chip (MCSoc-2018) (Hanoi, 12. September 2018 - 14. September 2018)
In: **Proceedings of Multicore/Many-core Systems-on-Chip (MCSoc-2018)** 2018
DOI: [10.1109/MCSoc2018.2018.00038](https://doi.org/10.1109/MCSoc2018.2018.00038)
BibTeX: [Download](#)
- Schwarzer T., Weichslgartner A., Glaß M., Wildermann S., Brand P., Teich J.:
[Symmetry-eliminating Design Space Exploration for Hybrid Application Mapping on Many-Core Architectures](#)
In: **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems** 37 (2018), p. 297-310
ISSN: 0278-0070
DOI: [10.1109/TCAD.2017.2695894](https://doi.org/10.1109/TCAD.2017.2695894)
BibTeX: [Download](#)
- Smirnov F., Reimann F., Teich J., Glaß M.:
[Automatic Optimization of the VLAN Partitioning in Automotive Communication Networks](#)
In: **ACM Transactions on Design Automation of Electronic Systems** (2018)
ISSN: 1084-4309
DOI: [10.1145/3278120](https://doi.org/10.1145/3278120)
BibTeX: [Download](#)
- Smirnov F., Reimann F., Teich J., Han Z., Glaß M.:
[Automatic Optimization of Redundant Message Routings in Automotive](#)

Networks

21st International Workshop on Software and Compilers for Embedded Systems (SCOPEs 2018) (Sankt Goar, 28. Mai 2018 - 30. Mai 2018)

In: ACM (ed.): **Proceedings of 21st International Workshop on Software and Compilers for Embedded Systems (SCOPEs 2018) 2018**

DOI: [10.1145/3207719.3207725](https://doi.org/10.1145/3207719.3207725)

BibTeX: [Download](#)

- Sousa É., Witterauf M., Brand M., Tanase AP., Hannig F., Teich J.:
[Invasive Computing for Predictability of Multiple Non-functional Properties: A Cyber-Physical System Case Study](#)
29th Annual IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP) (Milan, Italy, 10. Juli 2018 - 12. Juli 2018)
DOI: [10.1109/ASAP.2018.8445109](https://doi.org/10.1109/ASAP.2018.8445109)
URL: <https://ieeexplore.ieee.org/abstract/document/8445109/>
BibTeX: [Download](#)
- Streit FJ., Letras M., Wildermann S., Hackenberg B., [Falk J.](#), Becher A., Teich J.:
[Model-Based Design Automation of Hardware/Software Co-Designs for Xilinx Zynq PSoCs](#)
International Conference on Reconfigurable Computing and FPGAs (ReConFig) (Cancún, Mexico, 3. Dezember 2018 - 5. Dezember 2018)
In: **IEEE Proceedings of the 13th International Conference on ReConfigurable Computing and FPGAs 2018**
DOI: [10.1109/RECONFIG.2018.8641736](https://doi.org/10.1109/RECONFIG.2018.8641736)
BibTeX: [Download](#)
- Tanase AP., Hannig F., Teich J.:
[Symbolic Parallelization of Nested Loop Programs](#)
Springer, 2018
ISBN: 978-3-319-73908-3
DOI: [10.1007/978-3-319-73909-0](https://doi.org/10.1007/978-3-319-73909-0)
BibTeX: [Download](#)
- Weichslgartner A., Wildermann S., Gangadharan D., Glaß M., Teich J.:
[A Design-Time/Run-Time Application Mapping Methodology for Predictable Execution Time in MPSoCs](#)

In: **ACM Transactions on Embedded Computing Systems** (2018)

ISSN: 1539-9087

DOI: [10.1145/3274665](https://doi.org/10.1145/3274665)

BibTeX: [Download](#)

- Weichslgartner A., Wildermann S., Glaß M., Teich J.:

[Invasive Computing for Mapping Parallel Programs to Many-Core Architectures](#)

Springer, 2018

ISBN: 978-981-10-7355-7

DOI: [10.1007/978-981-10-7356-4](https://doi.org/10.1007/978-981-10-7356-4)

BibTeX: [Download](#)

- Witterauf M., Teich J.:

[Run-time Requirement Enforcement for Loop Programs on Processor Arrays](#)

16th ACM-IEEE International Conference on Formal Methods and Models for System Design (MEMOCODE) (Peking, 15. Oktober 2018 - 17. Oktober 2018)

In: ACM, IEEE (ed.): **Proceedings of the 16th ACM-IEEE International Conference on Formal Methods and Models for System Design (MEMOCODE) 2018**

DOI: [10.1109/MEMCOD.2018.8556911](https://doi.org/10.1109/MEMCOD.2018.8556911)

BibTeX: [Download](#)

- Ziener D., Pirkl J., Teich J.:

[Configuration Tempering of BRAM-based AES Implementations on FPGAs](#)

2018 International Conference on Reconfigurable Computing and FPGAs (Cancun, 3. Dezember 2018 - 5. Dezember 2018)

In: **Proceedings of 2018 International Conference on Reconfigurable Computing and FPGAs 2018**

DOI: [10.1109/reconfig.2018.8641692](https://doi.org/10.1109/reconfig.2018.8641692)

BibTeX: [Download](#)

- Özkan MA., Pérard-Gayot A., Membarth R., Slusallek P., Teich J., Hannig F.:

[A Journey into DSL Design using Generative Programming: FPGA Mapping of Image Border Handling through Refinement](#)

International Workshop on FPGAs for Software Programmers (Dublin, 31. August 2018)

2018)

In: **Proceedings of the Fifth International Workshop on FPGAs for Software Programmers 2018**

URL: <https://www12.cs.fau.de/downloads/oezkan/publications/fsp18.pdf>

BibTeX: [Download](#)

2017

- Aliee H., Banaiyanmofrad A., Glaß M., Teich J., Dutt N.:

[Redundancy-aware Design Space Exploration for Memory Reliability in Many-cores](#)

Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV'17) (Bremen, 8. Februar 2017 - 9. Februar 2017)

In: **Proc. Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV'17) 2017**

BibTeX: [Download](#)

- Aliee H., Borgonovo E., Glaß M., Teich J.:

[On the Boolean Extension of the Birnbaum Importance to Non-Coherent Systems](#)

In: **Reliability Engineering & System Safety** 160 (2017), p. 191-200

ISSN: 0951-8320

DOI: [10.1016/j.ress.2016.12.013](https://doi.org/10.1016/j.ress.2016.12.013)

BibTeX: [Download](#)

- Brand M., Hannig F., Tanase AP., Teich J.:

[Efficiency in ILP Processing by Using Orthogonality](#)

The 28th Annual IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP 2017) (Seattle, 10. Juli 2017 - 12. Juli 2017)

In: IEEE (ed.): **2017 IEEE 28th International Conference on Application-specific Systems, Architectures and Processors (ASAP) 2017**

DOI: [10.1109/ASAP.2017.7995282](https://doi.org/10.1109/ASAP.2017.7995282)

BibTeX: [Download](#)

- Brand M., Hannig F., Tanase AP., Teich J.:
[Orthogonal Instruction Processing: An Alternative to Lightweight VLIW Processors](#)
IEEE 11th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoc-17) (Korea University, Seoul, Korea, 18. September 2017 - 20. September 2017)
In: **2017 IEEE 11th International Symposium on Embedded Multicore/Many-core Systems-on-Chip 2017**
DOI: [10.1109/MCSoc.2017.17](https://doi.org/10.1109/MCSoc.2017.17)
BibTeX: [Download](#)
- Brand P., Ah Sue J., Brendel J., [Falk J.](#), Hasholzner R., Teich J., Wildermann S.:
[Exploiting Predictability in Dynamic Network Communication for Power-Efficient Data Transmission in LTE Radio Systems](#)
20th International Workshop on Software and Compilers for Embedded Systems (SCOPES'17) (Sankt Goar, Deutschland, 12. Juni 2017 - 13. Juni 2017)
In: ACM (ed.): **20th International Workshop on Software and Compilers for Embedded Systems (SCOPES'17) 2017**
DOI: [10.1145/3078659.3078670](https://doi.org/10.1145/3078659.3078670)
BibTeX: [Download](#)
- Echavarria Gutiérrez JA., Wildermann S., Potwigin E., Teich J.:
[Efficient Arithmetic Error Rate Calculus for Visibility Reduced Approximate Adders](#)
In: **IEEE Embedded Systems Letters** (2017), Article No.: 99
ISSN: 1943-0663
DOI: [10.1109/LES.2017.2760922](https://doi.org/10.1109/LES.2017.2760922)
BibTeX: [Download](#)
- [Falk J.](#), Haubelt C., Teich J., Zebelein C.:
[SystemoC: A Data-Flow Programming Language for Codesign](#)
In: Ha S, Teich J (ed.): **Handbook of Hardware/Software Codesign**, Dordrecht, The Netherlands: Springer, 2017, p. 59 - 97
ISBN: 978-94-017-7266-2
BibTeX: [Download](#)

- Fickenscher J., Bouzouraa ME., Hannig F., Teich J.:
[Environment Mapping Using Massively Parallel Architectures](#)
Vehicle Intelligence (München, 5. Dezember 2017 - 7. Dezember 2017)
BibTeX: [Download](#)
- Fickenscher J., Reinhart S., Bouzouraa ME., Hannig F., Teich J.:
[Convoy Tracking for ADAS on Embedded GPUs](#)
Intelligent Vehicles Symposium (IV 2017) (Redondo Beach, CA, USA, 11. Juni 2017 - 14. Juni 2017)
BibTeX: [Download](#)
- Glaß M., Teich J., Lukasiwycz M., Reimann F.:
[Hybrid Optimization Techniques for System-Level Design Space Exploration](#)
In: Ha S, Teich J (ed.): **Handbook of Hardware/Software Codesign**, Dordrecht, The Netherlands: Springer, 2017, p. 217-246
ISBN: 978-94-017-7266-2
BibTeX: [Download](#)
- Ha S., Teich J.:
[The Handbook of Hardware/Software Codesign](#)
Springer, 2017
DOI: [10.1007/978-94-017-7267-9_4](#)
BibTeX: [Download](#)
- Ha S., Teich J., Haubelt C., Glaß M., Mitra T., Dömer R., Eles P., Shrivastava A., Gerstlauer A., Bhattacharyya SS.:
[Introduction to Hardware/Software Codesign](#)
In: Ha S, Teich J (ed.): **Handbook of Hardware/Software Codesign**, Dordrecht, The Netherlands: Springer, 2017, p. 3-26
ISBN: 978-94-017-7266-2
DOI: [10.1007/978-94-017-7267-9](#)
BibTeX: [Download](#)
- Khdr H., Pagani S., Rodrigues Sousa E., Lari V., Pathania A., Hannig F., Shafique M., Teich J., Henkel J.:
[Power Density-Aware Resource Management for Heterogeneous Tiled Multi-cores](#)

In: **IEEE Transactions on Computers** 66 (2017), p. 488--501

ISSN: 0018-9340

DOI: [10.1109/TC.2016.2595560](https://doi.org/10.1109/TC.2016.2595560)

BibTeX: [Download](#)

- Khosravi F., Aliee H., Teich J.:

[System-Level Reliability Analysis Considering Imperfect Fault Coverage](#)

15th IEEE/ACM Symposium on Embedded Systems for Real-Time Multimedia (ESTIMedia) (Seoul, Republic of Korea, 15. Oktober 2017 - 20. Oktober 2017)

In: **15th IEEE/ACM Symposium on Embedded Systems for Real-Time Multimedia (ESTIMedia) 2017**

DOI: [10.1145/3139315.3141787](https://doi.org/10.1145/3139315.3141787)

BibTeX: [Download](#)

- Khosravi F., Glaß M., Teich J.:

[Automatic Reliability Analysis in the Presence of Probabilistic Common Cause Failures](#)

In: **IEEE Transactions on Reliability** 66 (2017), p. 319-338

ISSN: 0018-9529

DOI: [10.1109/TR.2016.2638320](https://doi.org/10.1109/TR.2016.2638320)

URL: <http://ieeexplore.ieee.org/document/7805166/>

BibTeX: [Download](#)

- Köstler H., Schmitt C., Kuckuk S., Kronawitter S., Hannig F., Teich J., Rüde U., Lengauer C.:

[A Scala Prototype to Generate Multigrid Solver Implementations for Different Problems and Target Multi-Core Platforms](#)

In: **International Journal of Computational Science and Engineering** 14 (2017), p. 150-163

ISSN: 1742-7185

DOI: [10.1504/IJCSE.2017.10003829](https://doi.org/10.1504/IJCSE.2017.10003829)

BibTeX: [Download](#)

- Letras M., [Falk J.](#), Wildermann S., Teich J.:

[Automatic Conversion of Simulink Models to SystemoC Actor Networks](#)

20th International Workshop on Software and Compilers for Embedded Systems (SCOPES) (Sankt Goar, 12. Juni 2017 - 13. Juni 2017)

DOI: [10.1145/3078659.3078668](https://doi.org/10.1145/3078659.3078668)

BibTeX: [Download](#)

- Li Z., Park H., Malik A., Wang Kl., Salcic Z., Kuzmin B., Glaß M., Teich J.:
[Using Design Space Exploration for Finding Schedules with Guaranteed Reaction Times of Synchronous Programs on Multi-core Architecture](#)
In: **Journal of Systems Architecture** 74 (2017), p. 30-45
ISSN: 1383-7621
BibTeX: [Download](#)
- Pirkl J., Becher A., Echavarria Gutiérrez JA., Teich J., Wildermann S.:
[Self-Adaptive FPGA-Based Image Processing Filters Using Approximate Arithmetics](#)
20th International Workshop on Software and Compilers for Embedded Systems (SCOPES) (Sankt Goar, 12. Juni 2017 - 13. Juni 2017)
In: **Proceedings of the 20th International Workshop on Software and Compilers for Embedded Systems 2017**
DOI: [10.1145/3078659.3078669](https://doi.org/10.1145/3078659.3078669)
BibTeX: [Download](#)
- Pourmohseni B., Glaß M., Teich J.:
[Automatic Operating Point Distillation for Hybrid Mapping Methodologies](#)
Design, Automation & Test in Europe Conference & Exhibition (DATE) (Lausanne, 27. März 2017 - 31. März 2017)
In: **Proceedings of the 20th Design, Automation & Test in Europe Conference & Exhibition (DATE) 2017**
DOI: [10.23919/DATE.2017.7927160](https://doi.org/10.23919/DATE.2017.7927160)
BibTeX: [Download](#)
- Pourmohseni B., Wildermann S., Glaß M., Teich J.:
[Predictable Run-Time Mapping Reconfiguration for Real-Time Applications on Many-Core Systems](#)
International Conference on Real-Time Networks and Systems (RTNS) (Grenoble, 4. Oktober 2017 - 6. Oktober 2017)
In: **Proceedings of the 25th International Conference on Real-Time Networks and Systems (RTNS) 2017**
DOI: [10.1145/3139258.3139278](https://doi.org/10.1145/3139258.3139278)

URL: <https://dl.acm.org/authorize?N42087>

BibTeX: [Download](#)

- Reiche O., Kobylko C., Hannig F., Teich J.:
[Auto-vectorization for Image Processing DSLs](#)
18th International Conference on Languages, Compilers, Tools, and Theory for Embedded Systems (LCTES) (Barcelona, 21. Juni 2017 - 22. Juni 2017)
In: **Proceedings of the 18th International Conference on Languages, Compilers, Tools, and Theory for Embedded Systems (LCTES) 2017**
DOI: [10.1145/3078633.3081039](https://doi.org/10.1145/3078633.3081039)
BibTeX: [Download](#)
- Reiche O., Özkan MA., Membarth R., Teich J., Hannig F.:
[Generating FPGA-based Image Processing Accelerators with Hipacc](#)
International Conference on Computer Aided Design (ICCAD) (Irvine, 13. November 2017 - 16. November 2017)
In: **Proceedings of the International Conference on Computer Aided Design (ICCAD) 2017**
DOI: [10.1109/ICCAD.2017.8203894](https://doi.org/10.1109/ICCAD.2017.8203894)
BibTeX: [Download](#)
- Roloff S., Hannig F., Teich J.:
[High Performance Network-on-Chip Simulation by Interval-based Timing Predictions](#)
15th IEEE/ACM Symposium on Embedded Systems for Real-Time Multimedia (ESTIMedia) (Seoul, Republic of Korea, 15. Oktober 2017 - 20. Oktober 2017)
In: ACM (ed.): **Proceedings of the 15th IEEE/ACM Symposium on Embedded Systems for Real-Time Multimedia (ESTIMedia) 2017**
DOI: [10.1145/3139315.3139320](https://doi.org/10.1145/3139315.3139320)
BibTeX: [Download](#)
- Schmidt B., Ziener D., Teich J., Zöllner C.:
[Optimizing Scrubbing by Netlist Analysis for FPGA Configuration Bit Classification and Floorplanning](#)
In: **Integration-The Vlsi Journal** (2017)
ISSN: 0167-9260
BibTeX: [Download](#)

- Smirnov F., Glaß M., Reimann F., Teich J.:
[Formal Timing Analysis of Non-Scheduled Traffic in Automotive Scheduled TSN Networks](#)
Design, Automation and Test in Europe (DATE) (Lausanne, 27. März 2017 - 30. März 2017)
In: **Proceedings of Design, Automation and Test in Europe (DATE) 2017**
2017
BibTeX: [Download](#)
- Smirnov F., Glaß M., Reimann F., Teich J.:
[Optimizing Message Routing and Scheduling in Automotive Mixed-Criticality Time-Triggered Networks](#)
54th ACM/EDAC/IEEE Design Automation Conference (DAC 2017) (Austin, 18. Juni 2017 - 22. Juni 2017)
In: **Proceedings of 54th ACM/EDAC/IEEE Design Automation Conference (DAC 2017) 2017**
DOI: [10.1145/3061639.3062298](#)
BibTeX: [Download](#)
- Sousa É., Chakraborty A., Tanase AP., Hannig F., Teich J.:
[TCPA Editor: A Design Automation Environment for a Class of Coarse-Grained Reconfigurable Arrays](#)
Demo Night at the IEEE International Conference on Reconfigurable Computing and FPGAs (ReConFig) (Cancun, Mexico, 4. Dezember 2017 - 6. Dezember 2017)
DOI: [10.1109/RECONFIG.2017.8279818](#)
URL: <http://ieeexplore.ieee.org/document/8279818/>
BibTeX: [Download](#)
- Sousa É., Tanase AP., Hannig F., Teich J.:
[A Reconfigurable Memory Architecture for System Integration of Coarse-Grained Reconfigurable Arrays](#)
International Conference on ReConFigurable Computing and FPGA's (ReConFig) (Cancun, Mexico, 4. Dezember 2017 - 6. Dezember 2017)
DOI: [10.1109/RECONFIG.2017.8279768](#)

URL: <http://ieeexplore.ieee.org/document/8279768/>

BibTeX: [Download](#)

- Streit FJ., Letras M., Schid M., [Falk J.](#), Wildermann S., Teich J.:
[**High-Level Synthesis for Hardware/Software Co-Design of Distributed Smart Camera Systems**](#)
International Conference on Distributed Smart Cameras (ICDSC) (Stanford, USA, 5. September 2017 - 7. September 2017)
In: **ACM Proceedings of the 11th International Conference on Distributed Smart Cameras 2017**
DOI: [10.1145/3131885.3131932](https://doi.org/10.1145/3131885.3131932)
BibTeX: [Download](#)
- Tanase AP., Witterauf M., Teich J., Hannig F.:
[**Symbolic Multi-Level Loop Mapping of Loop Programs for Massively Parallel Processor Arrays**](#)
In: **ACM Transactions on Embedded Computing Systems** 17 (2017), p. 31:1-31:27
ISSN: 1539-9087
DOI: [10.1145/3092952](https://doi.org/10.1145/3092952)
BibTeX: [Download](#)
- Teich J.:
[**Run-Time Monitoring and Enforcement of Non-functional Program Properties of Invasive Programs: Terms and Definitions**](#)
(2017)
URL: <https://www12.informatik.uni-erlangen.de/publications/pub2017/report-Teich17.pdf>
BibTeX: [Download](#)
(Techreport)
- Vogel-Heuser B., Wildermann S., Teich J.:
[**Towards the co-evolution of industrial products and its production systems by combining models from development and hardware/software deployment in cyber-physical systems**](#)
In: **Production Engineering** 11 (2017), p. 687-694
ISSN: 0944-6524

DOI: [10.1007/s11740-017-0765-0](https://doi.org/10.1007/s11740-017-0765-0)

BibTeX: [Download](#)

- Vogel-Heuser B., Wildermann S., Teich J.:

[**Towards the Co-Evolution of Industrial Products and its Production Systems by Combining Models from Development and Hardware/Software Deployment in Cyber-Physical Systems**](#)

In: **Production Engineering** 11 (2017), p. 687-694

ISSN: 0944-6524

DOI: [10.1007/s11740-017-0765-0](https://doi.org/10.1007/s11740-017-0765-0)

URL: <https://link.springer.com/article/10.1007/s11740-017-0765-0>

BibTeX: [Download](#)

- Witterauf M., Hannig F., Teich J.:

[**Constructing Fast and Cycle-Accurate Simulators for Configurable Accelerators Using C++ Templates**](#)

Symposium on Rapid System Prototyping (Seoul, South Korea, 19. Oktober 2017 - 20. Oktober 2017)

In: **Proceedings of the Symposium on Rapid System Prototyping 2017**

BibTeX: [Download](#)

- Zaib A., Heisswolf J., Weichslgartner A., Wild T., Teich J., Becker J., Herkersdorf A.:

[**Efficient Task Spawning for Shared Memory and Message Passing in Many-core Architectures**](#)

In: **Journal of Systems Architecture** 77 (2017), p. 72-82

ISSN: 1383-7621

DOI: [10.1016/j.sysarc.2017.03.004](https://doi.org/10.1016/j.sysarc.2017.03.004)

BibTeX: [Download](#)

- Özkan MA., Reiche O., Hannig F., Teich J.:

[**A Highly Efficient and Comprehensive Image Processing Library for C++-based High-Level Synthesis**](#)

Fourth International Workshop on FPGAs for Software Programmers (FSP) (Ghent, 7. September 2017)

In: **Proceedings of the Fourth International Workshop on FPGAs for Software Programmers (FSP) 2017**

URL: <https://ieeexplore.ieee.org/document/8084549>

BibTeX: [Download](#)

- Özkan MA., Reiche O., Hannig F., Teich J.:

[Hardware Design and Analysis of Efficient Loop Coarsening and Border Handling for Image Processing](#)

28th Annual IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP) (Seattle, 10. Juli 2017 - 12. Juli 2017)

In: **28th Annual IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP) 2017**

DOI: [10.1109/ASAP.2017.7995273](https://doi.org/10.1109/ASAP.2017.7995273)

URL: <https://www12.cs.fau.de/downloads/oezkan/publications/asap17.pdf>

BibTeX: [Download](#)

2016

- Ah Sue J., Hasholzner R., Brendel J., Kleinstauber M., Teich J.:

[A Binary Time Series Model of LTE Scheduling for Machine Learning Prediction](#)

10th IEEE International Conference on Self-Adaptive and Self-Organizing Systems (SASO 2016) (Augsburg, 12. September 2016 - 16. September 2016)

In: **1st International Workshops on Foundations and Applications of Self-Adaptive and Self-Organizing Systems (SASO 2016) Self-Organizing Systems (SASO 2016) 2016**

DOI: [10.1109/FAS-W.2016.64](https://doi.org/10.1109/FAS-W.2016.64)

BibTeX: [Download](#)

- Aliee H., Vitzethum S., Glaß M., Teich J., Borgonovo E.:

[Guiding Genetic Algorithms Using Importance Measures for Reliable Design of Embedded Systems](#)

29th IEEE Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (Connecticut, 19. September 2016 - 20. September 2016)

In: **Proceedings of 29th IEEE Symposium on Defect and Fault Tolerance in VLSI and 2016**

BibTeX: [Download](#)

- Becher A., Echavarria Gutiérrez JA., Ziener D., Wildermann S., Teich J.:
[**A LUT-Based Approximate Adder**](#)
24th Annual IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM 2016). (Washington DC, 1. Mai 2016 - 3. Mai 2016)
In: **Proceedings of the 24th Annual IEEE International Symposium on Field-Programmable Custom Computing Machines 2016**
DOI: [10.1109/FCCM.2016.16](https://doi.org/10.1109/FCCM.2016.16)
BibTeX: [Download](#)
- Becher A., Pirkl J., Herrmann A., Teich J., Wildermann S.:
[**Hybrid Energy-Aware Reconfiguration Management on Xilinx Zynq SoCs**](#)
International Conference on Reconfigurable Computing and FPGAs (ReConFig) (Cancún)
In: **Proceedings of the International Conference on Reconfigurable Computing and FPGAs (ReConFig) 2016**
DOI: [10.1109/ReConFig.2016.7857177](https://doi.org/10.1109/ReConFig.2016.7857177)
BibTeX: [Download](#)
- Becher A., Wildermann S., Mühlenthaler M., Teich J.:
[**ReOrder: Runtime Datapath Generation for High-Throughput Multi-Stream Processing**](#)
International Conference on Reconfigurable Computing and FPGAs (ReConFig) (Cancún)
In: **Proceedings of the International Conference on Reconfigurable Computing and FPGAs 2016**
DOI: [10.1109/ReConFig.2016.7857185](https://doi.org/10.1109/ReConFig.2016.7857185)
BibTeX: [Download](#)
- Bhadouria VS., Tanase AP., Schmid M., Hannig F., Teich J., Ghoshal D.:
[**A Novel Image Impulse Noise Removal Algorithm Optimized for Hardware Accelerators**](#)
In: **Journal of Signal Processing Systems** 89 (2016), p. 225-242
ISSN: 1939-8018
DOI: [10.1007/s11265-016-1187-5](https://doi.org/10.1007/s11265-016-1187-5)
BibTeX: [Download](#)

- Borgonovo E., Aliee H., Glaß M., Teich J.:
[**A New Time-Independent Reliability Importance Measure**](#)
In: **European Journal of Operational Research** (2016)
ISSN: 0377-2217
DOI: [10.1016/j.ejor.2016.03.054](https://doi.org/10.1016/j.ejor.2016.03.054)
BibTeX: [Download](#)
- Echavarria Gutiérrez JA., Wildermann S., Becher A., Teich J., Ziener D.:
[**FAU: Fast and Error-Optimized Approximate Adder Units on LUT-Based FPGAs**](#)
International Conference on Field Programmable Technology (FPT 2016) (Xi'an, 7. Dezember 2016 - 9. Dezember 2016)
In: **Proceedings of 2016 International Conference on Field Programmable Technology 2016**
DOI: [10.1109/FPT.2016.7929536](https://doi.org/10.1109/FPT.2016.7929536)
BibTeX: [Download](#)
- Fanucci L., Teich J.:
[**Proceedings of the 2016 Design, Automation & Test in Europe Conference & Exhibition, DATE 2016**](#)
In: **Proceedings of the 2016 Design, Automation & Test in Europe Conference & Exhibition, DATE 2016**, 2016
BibTeX: [Download](#)
- Fanucci L., Teich J.:
[**Recap of the 2016 DATE Conference & Exhibition**](#)
In: **IEEE Design and Test of Computers** 33 (2016), p. 114-117
ISSN: 0740-7475
DOI: [10.1109/MDAT.2016.2570223](https://doi.org/10.1109/MDAT.2016.2570223)
BibTeX: [Download](#)
- Fickenscher J., Reiche O., Schlumberger J., Hannig F., Teich J.:
[**Modeling, Programming and Performance Analysis of Automotive Environment Map Representations on Embedded GPUs**](#)
18th IEEE International High-Level Design Validation and Test Workshop (HLDVT) (Santa Cruz, CA, 7. Oktober 2016 - 8. Oktober 2016)
In: **Proceedings of the 18th IEEE International High-Level Design Validation**

and Test Workshop (HLDVT) 2016

DOI: [10.1109/HLDVT.2016.7748257](https://doi.org/10.1109/HLDVT.2016.7748257)

BibTeX: [Download](#)

- Hannig F., Cardoso J., Fey D., Schröder-Preikschat W., Teich J.:
[**Architecture of computing systems – ARCS 2016: 29th international conference Nuremberg, Germany, April 4-7, 2016 Proceedings**](#)
Springer Verlag, 2016
ISBN: 9783319306940
DOI: [10.1007/978-3-319-30695-7](https://doi.org/10.1007/978-3-319-30695-7)
BibTeX: [Download](#)
- Hannig F., Cardoso JMP., Pionteck T., Fey D., Schröder-Preikschat W., Teich J.:
[**Proceedings of the 29th International Conference on Architecture of Computing Systems \(ARCS\)**](#)
Berlin; Heidelberg: Springer-Verlag, 2016
(Lecture Notes in Computer Science (LNCS), Vol.9637)
ISBN: 978-3-319-30694-0
DOI: [10.1007/978-3-319-30695-7](https://doi.org/10.1007/978-3-319-30695-7)
BibTeX: [Download](#)
- Heißwolf J., Friederich S., Masing L., Weichslgartner A., Zaib A., Stein C., Duden M., Teich J., Herkersdorf A., Becker J.:
[**A Novel NoC-Architecture for Fault Tolerance and Power Saving**](#)
Third International Workshop on Multi-Objective Many-Core Design (MOMAC) in conjunction with International Conference on Architecture of Computing Systems (ARCS (Nuremberg, 4. April 2016 - 5. April 2016))
In: **In Proceedings of the third International Workshop on Multi-Objective Many-Core Design (MOMAC) in conjunction with International Conference on Architecture of Computing Systems (ARCS 2016)**
BibTeX: [Download](#)
- Herglotz C., Rosales R., Glaß M., Teich J., Kaup A.:
[**Multi-Objective Design Space Exploration for the Optimization of the HEVC Mode Decision Process**](#)
Picture Coding Symposium (PCS) (Nürnberg, 4. Dezember 2016 - 7. Dezember 2016)

In: **Picture Coding Symposium (PCS) 2016**

DOI: [10.1109/PCS.2016.7906327](https://doi.org/10.1109/PCS.2016.7906327)

URL: <http://arxiv.org/abs/2203.01782>

BibTeX: [Download](#)

- Häublein K., Reichenbach M., Reiche O., Özkan MA., Fey D., Hannig F., Teich J.:
[**Hybrid Code Description for Developing Fast and Resource Efficient Image Processing Architectures**](#)

16th International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS) (Island of Samos, 18. Juni 2016 - 21. Juni 2016)

In: **Proceedings of the 16th International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS) 2016**

DOI: [10.1109/SAMOS.2016.7818350](https://doi.org/10.1109/SAMOS.2016.7818350)

BibTeX: [Download](#)

- Lari V., Weichslgartner A., Tanase AP., Witterauf M., Khosravi F., Teich J., Heißwolf J., Friederich S., Becker J.:

[**Providing Fault Tolerance Through Invasive Computing**](#)

In: **it - Information Technology** 58 (2016), p. 309-238

ISSN: 1611-2776

BibTeX: [Download](#)

- Membarth R., Reiche O., Hannig F., Teich J., Körner M., Eckert W.:

[**HIPAcc: A Domain-Specific Language and Compiler for Image Processing**](#)

In: **IEEE Transactions on Parallel and Distributed Systems** 27 (2016), p. 210-224

ISSN: 1045-9219

DOI: [10.1109/TPDS.2015.2394802](https://doi.org/10.1109/TPDS.2015.2394802)

BibTeX: [Download](#)

- Mitra T., Teich J., Thiele L.:

[**Adaptive Isolation for Predictability and Security**](#)

2016

(Dagstuhl Reports, Vol.6)

BibTeX: [Download](#)

- Roloff S., Hannig F., Teich J.:
[InvadeSIM: A Simulator for Heterogeneous Multi-Processor Systems-on-Chip](#)
Design, Automation and Test in Europe (DATE) (Dresden, 14. März 2016 - 18. März 2016)
In: **Tool presentation at the University Booth 2016**
URL: <https://www.date-conference.com/system/files/file/date16/ubooth/37912.pdf>
BibTeX: [Download](#)
- Roloff S., Pöpl A., Schwarzer T., Wildermann S., Baader M., Glaß M., Hannig F., Teich J.:
[ActorX10: An Actor Library for X10](#)
ACM SIGPLAN X10 Workshop (X10), ACM (Santa Barbara, CA)
In: **Proceedings of the 6th ACM SIGPLAN X10 Workshop (X10) 2016**
BibTeX: [Download](#)
- Rosales R., Herglotz C., Glaß M., Teich J., Kaup A.:
[Analysis and Exploitation of CTU-Level Parallelism in the HEVC Mode Decision Process Using Actor-based Modeling](#)
Architecture of Computing Systems (ARCS) (Nürnberg, 4. April 2016 - 7. April 2016)
In: Springer (ed.): **In Proceedings of the International Conference on Architecture of Computing Systems (ARCS)**, Berlin; Heidelberg: 2016
DOI: [10.1007/978-3-319-30695-7_20](https://doi.org/10.1007/978-3-319-30695-7_20)
BibTeX: [Download](#)
- Salcic Z., Nadeem M., Park H., Teich J.:
[A heterogeneous multi-core SoC for mixed criticality industrial automation systems](#)
Emerging Technologies and Factory Automation (ETF A)
In: **Proceedings Emerging Technologies and Factory Automation (ETF A), 2016 IEEE 21st International Conference 2016**
BibTeX: [Download](#)
- Salcic Z., Nadeem M., Park H., Teich J.:
[Optimizing Latencies and Customizing NoC of Time-Predictable Heterogeneous Multi-Core Processor](#)

10th IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoc-16) (Lyon, 21. September 2016 - 23. September 2016)

In: **Proceedings of the 10th IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoc-16) 2016**

BibTeX: [Download](#)

- Schmid M., Reiche O., Hannig F., Teich J.:

[HIPAcc](#)

In: Dirk Koch, Frank Hannig, and Daniel Ziener (ed.): **FPGAs for Software Programmers**, Springer, 2016

DOI: [10.1007/978-3-319-26408-0_12](https://doi.org/10.1007/978-3-319-26408-0_12)

BibTeX: [Download](#)

- Schmitt C., Kuckuk S., Hannig F., Teich J., Köstler H., Rude U., Lengauer C.:

[Systems of Partial Differential Equations in ExaSlang](#)

In: **Software for Exascale Computing - SPPEXA 2013-2015**, Berlin, Heidelberg, New York: Springer, 2016, p. 47-67 (Lecture Notes in Computational Science and Engineering, Vol.113)

ISBN: 9783319405261

DOI: [10.1007/978-3-319-40528-5_3](https://doi.org/10.1007/978-3-319-40528-5_3)

BibTeX: [Download](#)

- Smirnov F., Glaß M., Reimann F., Teich J.:

[Formal Reliability Analysis of Switched Ethernet Automotive Networks under Transient Transmission Errors](#)

53rd ACM/EDAC/IEEE Design Automation Conference (DAC 2016) (Austin, 5. Juni 2016 - 9. Juni 2016)

In: **Proceedings of the 53rd ACM/EDAC/IEEE Design Automation Conference (DAC 2016) 2016**

BibTeX: [Download](#)

- Tanase AP., Witterauf M., Sousa É., Lari V., Hannig F., Teich J.:

[LoopInvader: A Compiler for Tightly Coupled Processor Arrays](#)

Design, Automation and Test in Europe (DATE) (Dresden, 14. März 2016 - 18. März 2016)

In: **Tool presentation at the University Booth 2016**

URL: <https://www.date-conference.com/system/files/file/date16/ubooth/37913.pdf>

BibTeX: [Download](#)

- Teich J.:

[**Invasive Computing - Editorial**](#)

In: **it - Information Technology** 58 (2016), p. 263-265

ISSN: 1611-2776

BibTeX: [Download](#)

- Teich J., Glaß M., Roloff S., Schröder-Preikschat W., Snelting G., Weichslgartner A., Wildermann S.:

[**Language and Compilation of Parallel Programs for *-Predictable MPSoC Execution using Invasive Computing**](#)

10th IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoc-16) (Lyon, 21. September 2016 - 23. September 2016)

In: **Proceedings of the 10th IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoc-16) 2016**

DOI: [10.1109/MCSoc.2016.30](https://doi.org/10.1109/MCSoc.2016.30)

BibTeX: [Download](#)

- Wang B., Xu Y., Hasholzner R., Drewes C., Rosales R., Graf S., [Falk J.](#), Glaß M., Teich J.:

[**Exploration of Power Domain Partitioning for Application-Specific SoCs in System-Level Design**](#)

19. GI/ITG/GMM-Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV 2016) (Freiburg, 1. März 2016 - 2. März 2016)

In: **In Proceedings of the 19. GI/ITG/GMM-Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV 2016) 2016**

DOI: [10.6094/UNIFR/10643](https://doi.org/10.6094/UNIFR/10643)

BibTeX: [Download](#)

- Weichslgartner A., Teich J.:

[**Position Paper: Towards Redundant Communication through Hybrid Application Mapping**](#)

Third International Workshop on Multi-Objective Many-Core Design (MOMAC) in

in conjunction with International Conference on Architecture of Computing Systems (ARCS) (Nuremberg, 4. April 2016 - 5. April 2016)

In: **Proceedings of the third International Workshop on Multi-Objective Many-Core Design (MOMAC) in conjunction with International Conference on Architecture of Computing Systems (ARCS) 2016**

BibTeX: [Download](#)

- Weichslgartner A., Wildermann S., Götzfried J., Freiling F., Glaß M., Teich J.:
[**Design-Time/Run-Time Mapping of Security-Critical Applications in Heterogeneous MPSoCs**](#)

19th International Workshop on Software and Compilers for Embedded Systems (SCOPES) (St. Goar, 23. Mai 2016 - 25. Mai 2016)

In: **In Proceedings of the 19th International Workshop on Software and Compilers for Embedded Systems (SCOPES) 2016**

DOI: [10.1145/2906363.2906370](https://doi.org/10.1145/2906363.2906370)

BibTeX: [Download](#)

- Wildermann S., Bader M., Bauer L., Damschen M., Gabriel D., Gerndt M., Glaß M., Henkel J., Paul J., Pöppel A., Roloff S., Schwarzer T., Snelting G., Stechele W., Teich J., Weichslgartner A., Zwinkau A.:

[**Invasive Computing for Timing-Predictable Stream Processing on MPSoCs**](#)

In: **it - Information Technology** 58 (2016), p. 267-280

ISSN: 1611-2776

DOI: [10.1515/itit-2016-0021](https://doi.org/10.1515/itit-2016-0021)

BibTeX: [Download](#)

- Witterauf M., Tanase AP., Hannig F., Teich J.:
[**Modulo Scheduling of Symbolically Tiled Loops for Tightly Coupled Processor Arrays**](#)

IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP) (London, 6. Juli 2016 - 8. Juli 2016)

In: **Proceedings of the 27th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP) 2016**

BibTeX: [Download](#)

- Xu Y., Teich J.:
[**Hierarchical Statistical Leakage Analysis and its Application**](#)

In: **ACM Transactions on Design Automation of Electronic Systems** (2016)

ISSN: 1084-4309

BibTeX: [Download](#)

- Ziener D., Weber H., Vogt JS., Schürfeld U., Meyer-Wegener K., Teich J., Dennl C., Becher A., Bauer F.:

[FPGA-Based Dynamically Reconfigurable SQL Query Processing](#)

In: **ACM Transactions on Reconfigurable Technology and Systems** 9 (2016),
p. 25:1-25:24

ISSN: 1936-7406

DOI: [10.1145/2845087](https://doi.org/10.1145/2845087)

BibTeX: [Download](#)

- Özkan MA., Reiche O., Hannig F., Teich J.:

[FPGA-Based Accelerator Design from a Domain-Specific Language](#)

26th International Conference on Field-Programmable Logic and Applications (FPL) (Lausanne, 29. August 2016 - 2. September 2016)

In: **Proceedings of the 26th International Conference on Field-Programmable Logic and Applications (FPL) 2016**

DOI: [10.1109/FPL.2016.7577357](https://doi.org/10.1109/FPL.2016.7577357)

BibTeX: [Download](#)

2015

- Aliee H., Borgonovo E., Glaß M., Teich J.:

[Importance measures in time-dependent reliability analysis and system design](#)

25th European Safety and Reliability Conference, ESREL 2015 (Zürich, 7. September 2015 - 10. September 2015)

In: **Proceedings of the Annual European Safety and Reliability Conference (ESREL '15) 2015**

URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=84959018237&origin=inward>

BibTeX: [Download](#)

- Aliee H., Glaß M., Chen L., Ebrahimi M., Khosravi F., Kleeberger VB., Listl A., Müller-Gritschneider D., Oboril F., Schlichtmann U., Tahoori MB., Teich J., Wehn

N., Weis C.:

[Application-aware cross-layer reliability analysis and optimization](#)

In: **it - Information Technology** 57 (2015), p. 159-169

ISSN: 1611-2776

DOI: [10.1515/itit-2014-1080](https://doi.org/10.1515/itit-2014-1080)

BibTeX: [Download](#)

- Becher A., Echavarria Gutiérrez JA., Ziener D., Teich J.:

[Approximate Adder Structures on FPGAs](#)

AxC15: 1st Workshop on Approximate Computing (Paderborn, Germany)

Open Access: [https://www12.cs.fau.de/downloads/echavarria/pub/Approximate Adder Structures on FPGAs.pdf](https://www12.cs.fau.de/downloads/echavarria/pub/Approximate%20Adder%20Structures%20on%20FPGAs.pdf)

BibTeX: [Download](#)

- Becher A., Ziener D., Meyer-Wegener K., Teich J.:

[A co-design approach for accelerated SQL query processing via FPGA-based data filtering](#)

International Conference on Field Programmable Technology, FPT 2015 (Queenstown, 7. Dezember 2015 - 9. Dezember 2015)

DOI: [10.1109/FPT.2015.7393148](https://doi.org/10.1109/FPT.2015.7393148)

BibTeX: [Download](#)

- [Falk J.](#), Schwarzer T., Glaß M., Teich J., Zebelein C., Haubelt C.:

[Quasi-static scheduling of data flow graphs in the presence of limited channel capacities](#)

13th IEEE Symposium on Embedded Systems for Real-Time Multimedia, ESTI-Media 2015

DOI: [10.1109/ESTIMedia.2015.7351766](https://doi.org/10.1109/ESTIMedia.2015.7351766)

BibTeX: [Download](#)

- [Falk J.](#), Schwarzer T., Zhang L., Glaß M., Teich J.:

[Automatic communication-driven virtual prototyping and design for networked embedded systems](#)

In: **Microprocessors and Microsystems** 39 (2015), p. 1012–1028

ISSN: 0141-9331

DOI: [10.1016/j.micpro.2015.08.008](https://doi.org/10.1016/j.micpro.2015.08.008)

BibTeX: [Download](#)

- Gangadharan D., Sousa É., Lari V., Hannig F., Teich J.:
[Application-driven reconfiguration of shared resources for timing predictability of MPSoC platforms](#)
48th Asilomar Conference on Signals, Systems and Computers, ACSSC 2015 (Pacific Grove, CA, 2. November 2014 - 5. November 2014)
In: **Proceedings of Asilomar Conference on Signals, Systems, and Computers (ASILOMAR) 2015**
DOI: [10.1109/ACSSC.2014.7094471](https://doi.org/10.1109/ACSSC.2014.7094471)
BibTeX: [Download](#)
- Glein R., Rittner F., Becher A., Ziener D., Frickel J., Teich J., Heuberger A.:
[Reliability of Space-Grade vs. COTS SRAM-Based FPGA in N-Modular Redundancy](#)
2015 NASA/ESA Conference on Adaptive Hardware and Systems (Montreal, 15. Juni 2015 - 18. Juni 2015)
In: IEEE (ed.): **Proceedings of 2015 NASA/ESA Conference on Adaptive Hardware and Systems 2015**
BibTeX: [Download](#)
- Graf S., Glaß M., Teich J.:
[Symbolic Message Routing for Multi-Objective Optimization of Automotive E/E Architecture Component Platforms](#)
18. Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV 2015) (Chemnitz, 3. März 2015 - 4. März 2015)
In: **Proceedings of 18. Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV 2015) 2015**
BibTeX: [Download](#)
- Graf S., Glaß M., Teich J., Platte D.:
[A Methodology for the Optimized Design of an E/E Architecture Component Platform](#)
Stuttgart International Symposium (Stuttgart, 17. März 2015 - 18. März 2015)
In: **Proceedings of the Stuttgart International Symposium 2015**

DOI: [10.1007/978-3-658-08844-6_14](https://doi.org/10.1007/978-3-658-08844-6_14)

BibTeX: [Download](#)

- Graf S., Reinhart S., Glaß M., Teich J., Platte D.:
[Robust Design of E/E Architecture Component Platforms](#)
52nd ACM/EDAC/IEEE Design Automation Conference (DAC 2015) (San Francisco, CA, 7. Juni 2015 - 11. Juni 2015)
In: **Proceedings of the 52nd ACM/EDAC/IEEE Design Automation Conference (DAC 2015)** 2015
DOI: [10.1145/2744769.2747941](https://doi.org/10.1145/2744769.2747941)
BibTeX: [Download](#)
- Heißwolf J., Weichslgartner A., Zaib A., Friederich S., Masing L., Stein C., Duden M., Klöpfer R., Teich J., Wild T., Herkersdorf A., Becker J.:
[Fault-tolerant communication in invasive networks on chip](#)
NASA/ESA Conference on Adaptive Hardware and Systems, AHS 2015
In: **Proceedings of the 2015 NASA/ESA Conference on Adaptive Hardware and Systems (AHS)** 2015
DOI: [10.1109/AHS.2015.7231156](https://doi.org/10.1109/AHS.2015.7231156)
BibTeX: [Download](#)
- Khosravi F., Müller M., Glaß M., Teich J.:
[Uncertainty-aware reliability analysis and optimization](#)
2015 Design, Automation and Test in Europe Conference and Exhibition, DATE 2015 (Grenoble, 9. März 2015 - 13. März 2015)
In: **Proceedings of Design, Automation and Test in Europe (DATE 2015)** 2015
DOI: [10.7873/DATE.2015.0319](https://doi.org/10.7873/DATE.2015.0319)
BibTeX: [Download](#)
- Lari V., Tanase AP., Teich J., Witterauf M., Khosravi F., Hannig F., Meyer B.:
[A co-design approach for fault-tolerant loop execution on Coarse-Grained Reconfigurable Arrays](#)
NASA/ESA Conference on Adaptive Hardware and Systems, AHS 2015 (Montreal, 15. Juni 2016 - 18. Juni 2015)
In: **Proceedings of the 2015 NASA/ESA Conference on Adaptive Hardware and Systems** 2015

DOI: [10.1109/AHS.2015.7231157](https://doi.org/10.1109/AHS.2015.7231157)

BibTeX: [Download](#)

- Paul J., Stechele W., Oechslein B., Erhardt C., Schedel J., Lohmann D., Schröder-Preikschat W., Kröhnert M., Asfour T., Sousa É., Hannig F., Lari V., Teich J., Grudnitsky A., Bauer L., Henkel J.:

[Resource-awareness on heterogeneous MPSoCs for image processing](#)

In: **Journal of Systems Architecture** 61 (2015), p. 668-680

ISSN: 1383-7621

DOI: [10.1016/j.sysarc.2015.09.002](https://doi.org/10.1016/j.sysarc.2015.09.002)

BibTeX: [Download](#)

- Reiche O., Häublein K., Reichenbach M., Hannig F., Teich J., Fey D.:
[Automatic Optimization of Hardware Accelerators for Image Processing](#)
DATE Friday Workshop on Heterogeneous Architectures and Design Methods for Embedded Image Systems (HIS 2015) (Grenoble, 13. März 2015 - 13. März 2015)

In: **Proceedings of the DATE Friday Workshop on Heterogeneous Architectures and Design Methods for Embedded Image Systems (HIS 2015) 2015**

URL: <http://arxiv.org/abs/1502.07448>

BibTeX: [Download](#)

- Reiche O., Häublein K., Reichenbach M., Schmid M., Hannig F., Teich J., Fey D.:
[Synthesis and Optimization of Image Processing Accelerators using Domain Knowledge](#)

In: **Journal of Systems Architecture** 61 (2015), p. 646-658

ISSN: 1383-7621

DOI: [10.1016/j.sysarc.2015.09.004](https://doi.org/10.1016/j.sysarc.2015.09.004)

URL: <https://www12.cs.fau.de/downloads/reiche/publications/RHRSHTF15.pdf>

BibTeX: [Download](#)

- Roloff S., Schafhauser D., Hannig F., Teich J.:
[Execution-driven parallel simulation of PGAS applications on heterogeneous tiled architectures](#)

52nd ACM/EDAC/IEEE Design Automation Conference, DAC 2015 (San Francisco, CA, 7. Juni 2015 - 11. Juni 2015)

In: **Proceedings of the 52nd ACM/EDAC/IEEE Design Automation Conference (DAC) 2015**

DOI: [10.1145/2744769.2744840](https://doi.org/10.1145/2744769.2744840)

BibTeX: [Download](#)

- Roloff S., Wildermann S., Hannig F., Teich J.:

[Invasive computing for predictable stream processing: A simulation-based case study](#)

13th IEEE Symposium on Embedded Systems for Real-Time Multimedia, ESTI-Media 2015 (Amsterdam, 8. Oktober 2015 - 9. Oktober 2015)

DOI: [10.1109/ESTIMedia.2015.7351761](https://doi.org/10.1109/ESTIMedia.2015.7351761)

BibTeX: [Download](#)

- Schmid M., Reiche O., Hannig F., Teich J.:

[Loop Coarsening in C-based High-Level Synthesis](#)

26th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP) (Toronto, 27. Juli 2015 - 29. Juli 2015)

In: **Proceedings of the 26th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP) 2015**

DOI: [10.1109/ASAP.2015.7245730](https://doi.org/10.1109/ASAP.2015.7245730)

URL: <https://www12.cs.fau.de/downloads/reiche/publications/SRHT15.pdf>

BibTeX: [Download](#)

- Schmitt C., Schmid M., Hannig F., Teich J., Kuckuk S., Köstler H.:

[Generation of Multigrid-based Numerical Solvers for FPGA Accelerators](#)

2nd International Workshop on High-Performance Stencil Computations (HiStencils) (Amsterdam, 20. Januar 2015 - 20. Januar 2015)

In: **Proceedings of the 2nd International Workshop on High-Performance Stencil Computations (HiStencils) 2015**

URL: <https://www12.cs.fau.de/downloads/schmittch/publications/SSHTKK15his-tencils.pdf>

BibTeX: [Download](#)

- Schwarzer T., [Falk J.](#), Glaß M., Teich J., Zebelein C., Haubelt C.:

[Throughput-optimizing compilation of dataflow applications for multi-cores using quasi-static scheduling](#)

18th International Workshop on Software and Compilers for Embedded Systems,

SCOPES 2015 (St. Goar)

In: **Proceedings of the 18th International Workshop on Software and Compilers for Embedded Systems (SCOPES) 2015**

DOI: [10.1145/2764967.2764972](https://doi.org/10.1145/2764967.2764972)

BibTeX: [Download](#)

- Seyler J., Navet N., Fejoz L., Teich J.:
[Insights on the Configuration and Performances of SOME/IP Service Discovery](#)
In: **SAE International Journal of Passenger Cars - Electronic and Electrical Systems** 8 (2015), p. 124-129
ISSN: 1946-4614
BibTeX: [Download](#)
- Seyler J., Streichert T., Glaß M., Navet N., Teich J.:
[Formal analysis of the startup delay of SOME/IP service discovery](#)
2015 Design, Automation and Test in Europe Conference and Exhibition, DATE 2015 (Grenoble, 9. März 2015 - 13. März 2015)
In: **Proceedings of Design, Automation and Test in Europe (DATE 2015) 2015**
DOI: [10.7873/DATE.2015.0469](https://doi.org/10.7873/DATE.2015.0469)
BibTeX: [Download](#)
- Sousa É., Hannig F., Teich J.:
[Reconfigurable Buffer Structures for Coarse-Grained Reconfigurable Arrays](#)
International Embedded Systems Symposium (IESS) (Foz do Iguaçu, 3. November 2015 - 6. November 2015)
In: Marcelo Götz, Gunar Schirner, Marco Aurélio Wehrmeister, Mohammad Abdullah Al Faruque, and Achim Rettberg (ed.): **Proceedings of the International Embedded Systems Symposium (IESS) 2015**
DOI: [10.1007/978-3-319-90023-0](https://doi.org/10.1007/978-3-319-90023-0)
URL: <http://www.springer.com/us/book/9783319900223>
BibTeX: [Download](#)
- Sousa É., Hannig F., Teich J., Schlichtmann U., Chen Q.:
[Runtime adaptation of application execution under thermal and power constraints in massively parallel processor arrays](#)

18th International Workshop on Software and Compilers for Embedded Systems, SCOPES 2015 (St. Goar, 1. Juni 2015 - 3. Juni 2015)

In: **In Proceedings of the 18th International Workshop on Software and Compilers for Embedded Systems (SCOPES) 2015**

DOI: [10.1145/2764967.2771933](https://doi.org/10.1145/2764967.2771933)

BibTeX: [Download](#)

- Tanase AP., Witterauf M., Hannig F., Teich J.:

[Symbolic loop parallelization for balancing I/O and memory accesses on processor arrays](#)

ACM/IEEE International Conference on Formal Methods and Models for Code-sign, MEMOCODE 2015 (Austin, 21. September 2015 - 23. September 2015)

In: **Proceedings of the 13th ACM-IEEE International Conference on Formal Methods and Models for System Design (MEMOCODE) 2015**

DOI: [10.1109/MEMCOD.2015.7340486](https://doi.org/10.1109/MEMCOD.2015.7340486)

BibTeX: [Download](#)

- Tanase AP., Witterauf M., Teich J., Hannig F., Lari V.:

[On-demand fault-tolerant loop processing on massively parallel processor arrays](#)

26th IEEE International Conference on Application-Specific Systems, Architectures and Processors, ASAP 2015 (Toronto, 27. Juli 2015 - 29. Juli 2015)

In: **In Proceedings of the 26th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP) 2015**

DOI: [10.1109/ASAP.2015.7245734](https://doi.org/10.1109/ASAP.2015.7245734)

BibTeX: [Download](#)

- Teich J.:

[Adaptive Isolation for Predictable MPSoC Stream Processing](#)

18th Int. Workshop on Software and Compilers for Embedded Systems (SCOPES 2015) (Schloss Rheinfels, St. Goar, 1. Juni 2015 - 3. Juni 2015)

In: **Proc. of the 18th Int. Workshop on Software and Compilers for Embedded Systems (SCOPES 2015) 2015**

DOI: [10.1145/2764967.2771821](https://doi.org/10.1145/2764967.2771821)

BibTeX: [Download](#)

- Teich J., Boppu S., Hannig F., Lari V.:
[Compact Code Generation and Throughput Optimization for Coarse-Grained Reconfigurable Arrays](#)
In: Luk, Wayne, Constantinides, George A. (ed.): **Transforming Reconfigurable Systems: A Festschrift Celebrating the 60th Birthday of Professor Peter Cheung**, 2015, p. 167-206
ISBN: 978-1-78326-696-8
DOI: [10.1142/9781783266975_0010](https://doi.org/10.1142/9781783266975_0010)
BibTeX: [Download](#)
- Teich J., Lari V., Tanase AP., Witterauf M., Khosravi F., Meyer B.:
[Techniques for on-demand structural redundancy for massively parallel processor arrays](#)
In: **Journal of Systems Architecture** 61 (2015), p. 615-627
ISSN: 1383-7621
DOI: [10.1016/j.sysarc.2015.10.004](https://doi.org/10.1016/j.sysarc.2015.10.004)
BibTeX: [Download](#)
- Weichslgartner A., Heißwolf J., Zaib A., Wild T., Herkersdorf A., Becker J., Teich J.:
[Position Paper: Towards Hardware-Assisted Decentralized Mapping of Applications for Heterogeneous NoC Architectures.](#)
International Workshop on Multi-Objective Many-Core Design (MOMAC) in conjunction with International Conference on Architecture of Computing Systems (ARCS) (Porto, 24. März 2015 - 24. März 2015)
In: **Proceedings of the second International Workshop on Multi-Objective Many-Core Design (MOMAC) in conjunction with International Conference on Architecture of Computing Systems (ARCS) 2015**
BibTeX: [Download](#)
- Wildermann S., Weichslgartner A., Teich J.:
[Design Methodology and Run-Time Management for Predictable Many-Core Systems](#)
18th IEEE International Symposium on Real-Time Distributed Computing Workshops, ISORCW 2015 (Auckland)
In: **Proceedings of the 6th IEEE Workshop on Self-Organizing Real-Time**

Systems (SORT 2015) 2015

DOI: [10.1109/ISORCW.2015.48](https://doi.org/10.1109/ISORCW.2015.48)

BibTeX: [Download](#)

- Witterauf M., Tanase AP., Hannig F., Teich J.:
[**Adaptive Fault Tolerance in Tightly Coupled Processor Arrays with Invasive Computing**](#)
11th International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems (ACACES) (Fiuggi, 12. Juli 2015 - 18. Juli 2015)
In: **Proceedings of the 11th International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems (ACACES) 2015**
BibTeX: [Download](#)
- Witterauf M., Tanase AP., Teich J., Lari V., Zwinkau A., Snelting G.:
[**Adaptive fault tolerance through invasive computing**](#)
NASA/ESA Conference on Adaptive Hardware and Systems, AHS 2015 (Montreal, 15. Juni 2016 - 18. Juni 2015)
In: **Proceedings of the 2015 NASA/ESA Conference on Adaptive Hardware and Systems 2015**
DOI: [10.1109/AHS.2015.7231155](https://doi.org/10.1109/AHS.2015.7231155)
BibTeX: [Download](#)
- Zaib A., Heißwolf J., Weichslgartner A., Wild T., Teich J., Becker J., Herkersdorf A.:
[**Network interface with task spawning support for NoC-based DSM architectures**](#)
28th International Conference on Architecture of Computing Systems, ARCS 2015 (Porto, 24. März 2015 - 24. März 2015)
In: **Proceedings of 28th GI/ITG International Conference on Architecture of Computing Systems (ARCS) 2015**
DOI: [10.1007/978-3-319-16086-3_15](https://doi.org/10.1007/978-3-319-16086-3_15)
BibTeX: [Download](#)

- Zhang L., Glaß M., Ballmann N., Teich J.:
[Bridging Algorithm and ESL Design: MATLAB/Simulink Model Transformation and Validation](#)
In: Marie-Minerve Louërat, Torsten Maehne (ed.): **Languages, Design Methods, and Tools for Electronic System Design**, Springer, 2015, p. 189-206
ISBN: 978-3-319-06316-4
DOI: [10.1007/978-3-319-06317-1_10](https://doi.org/10.1007/978-3-319-06317-1_10)
BibTeX: [Download](#)
- Ziener D., Bauer F., Becher A., Dennl C., Meyer-Wegener K., Schürfeld U., Teich J., Vogt JS., Weber H.:
[FPGA-Based Dynamically Reconfigurable SQL Query Processing](#)
In: **ACM Transactions on Reconfigurable Technology and Systems** (2015)
ISSN: 1936-7406
BibTeX: [Download](#)

2014

- Abelein U., Cook A., Engelke P., Glaß M., Reimann F., Gómez LR., Russ T., Teich J., Ull D., Wunderlich HJ.:
[Non-Intrusive Integration of Advanced Diagnosis Features in Automotive E/E-Architectures](#)
Design, Automation and Test in Europe (DATE) (Dresden, 24. März 2014 - 28. März 2014)
In: **Proc. of Design, Automation and Test in Europe (DATE)**, New York, NY, USA: 2014
DOI: [10.7873/DATE2014.373](https://doi.org/10.7873/DATE2014.373)
BibTeX: [Download](#)
- Aliee H., Glaß M., Khosravi F., Teich J.:
[An efficient technique for computing importance measures in automatic design of dependable embedded systems](#)
2014 International Conference on Hardware/Software Codesign and System Synthesis, CODES+ISSS 2014 (New Delhi, 12. Oktober 2014 - 17. Oktober 2014)
In: **Proceedings of the International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS 2014) 2014**

DOI: [10.1145/2656075.2656079](https://doi.org/10.1145/2656075.2656079)

BibTeX: [Download](#)

- Aliee H., Glaß M., [Wanka R.](#), Teich J.:
[Automatic Graph-based Success Tree Construction and Analysis](#)
Annual Reliability and Maintainability Symposium (RAMS) (Colorado Springs, Colorado, USA, 27. Januar 2014 - 30. Januar 2014)
In: **Proc. 60th Annual Reliability and Maintainability Symposium (RAMS) 2014**
DOI: [10.1109/RAMS.2014.6798487](https://doi.org/10.1109/RAMS.2014.6798487)
URL: <https://www12.informatik.uni-erlangen.de/people/rwanka/publications/AGWT14.php>
BibTeX: [Download](#)
- Becher A., Bauer F., Ziener D., Teich J.:
[Energy-aware SQL query acceleration through FPGA-based dynamic partial reconfiguration](#)
24th International Conference on Field Programmable Logic and Applications, FPL 2014 (Munich, 2. September 2014 - 4. September 2014)
In: **Proceedings of the Conference on Field-Programmable Logic and Applications (FPL 2014) 2014**
DOI: [10.1109/FPL.2014.6927502](https://doi.org/10.1109/FPL.2014.6927502)
BibTeX: [Download](#)
- Boppu S., Hannig F., Teich J.:
[Compact Code Generation for Tightly-Coupled Processor Arrays](#)
In: **Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology** 77(1-2) (2014), p. 5-29
ISSN: 1387-5485
DOI: [10.1007/s11265-014-0891-2](https://doi.org/10.1007/s11265-014-0891-2)
BibTeX: [Download](#)
- Gangadharan D., Tanase AP., Hannig F., Teich J.:
[Timing Analysis of a Heterogeneous Architecture with Massively Parallel Processor Arrays](#)
DATE Friday Workshop on Performance, Power and Predictability of Many-Core Embedded Systems (3PMCES) (Dresden, Germany, 28. März 2014 - 28. März

2014)

URL: <https://ecsi.org/resource/workshop/2014/3PMCES/DATE/paper/timing-analysis-heterogeneous-architecture-massively-parallel-processor-arrays>

BibTeX: [Download](#)

- Gangadharan D., Teich J., Chakraborty S.:
[Quality-aware video decoding on thermally-constrained MPSoC platforms](#)
25th IEEE International Conference on Application-Specific Systems, Architectures and Processors, ASAP 2014 (Zurich, 18. Juni 2014 - 29. Juni 2014)
In: **Proceedings of the 25th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP) 2014**
DOI: [10.1109/ASAP.2014.6868670](https://doi.org/10.1109/ASAP.2014.6868670)
BibTeX: [Download](#)
- Glaß M., Graf S., Reimann F., Teich J.:
[Design and Evaluation of Future Ethernet AVB-based ECU Networks](#)
In: **Embedded Systems Development, From Functional Models to Implementations 2014**, Berlin; Heidelberg: Springer-Verlag, 2014, p. 205-220
ISBN: 978-1-4614-3878-6
BibTeX: [Download](#)
- Glein R., Schmidt B., Rittner F., Teich J., Ziener D.:
[A self-adaptive SEU mitigation system for FPGAs with an internal block RAM radiation particle sensor](#)
22nd IEEE International Symposium on Field-Programmable Custom Computing Machines, FCCM 2014 (Boston, 11. Mai 2014 - 13. Mai 2014)
In: **Proceedings of Field-Programmable Custom Computing Machines (FCCM 2014) 2014**
DOI: [10.1109/FCCM.2014.79](https://doi.org/10.1109/FCCM.2014.79)
BibTeX: [Download](#)
- Glocker E., Boppu S., Chen Q., Schlichtmann U., Teich J., Schmitt-Landsiedel D.:
[Temperature modeling and emulation of an ASIC temperature monitor system for Tightly-Coupled Processor Arrays \(TCPAs\)](#)
In: **Advances in Radio Science** 12 (2014), p. 103-109
ISSN: 1684-9973

DOI: [10.5194/ars-12-103-2014](https://doi.org/10.5194/ars-12-103-2014)

BibTeX: [Download](#)

- Graf S., Glaß M., Teich J., Lauer C.:
[Design Space Exploration for Automotive E/E Architecture Component Platforms](#)
Euromicro Conference on Digital System Design (DSD) (Verona, 27. August 2014 - 29. August 2014)
In: **Proc. of Euromicro Conference on Digital System Design (DSD)**, New York, NY, USA: 2014
DOI: [10.1109/DSD.2014.43](https://doi.org/10.1109/DSD.2014.43)
BibTeX: [Download](#)
- Graf S., Glaß M., Teich J., Lauer C.:
[Multi-Variant-based Design Space Exploration for Automotive Embedded Systems](#)
Design, Automation and Test in Europe (DATE) (Dresden, 24. März 2014 - 28. März 2014)
In: **Proc. of Design, Automation and Test in Europe (DATE)**, New York, NY, USA: 2014
DOI: [10.7873/DATE2014.020](https://doi.org/10.7873/DATE2014.020)
BibTeX: [Download](#)
- Graf S., Reimann F., Glaß M., Teich J.:
[Towards Scalable Symbolic Routing for Multi-Objective Networked Embedded System Design and Optimization](#)
International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) (New Delhi, 12. Oktober 2014 - 17. Oktober 2014)
In: **Proc. of the International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)**, New York, NY, USA: 2014
DOI: [10.1145/2656075.2656102](https://doi.org/10.1145/2656075.2656102)
BibTeX: [Download](#)
- Grebhahn A., Kuckuk S., Schmitt C., Köstler H., Siegmund N., Apel S., Hannig F., Teich J.:
[Experiments on Optimizing the Performance of Stencil Codes with SPL Conqueror](#)

In: **Parallel Processing Letters** 24 (2014)

ISSN: 0129-6264

DOI: [10.1142/S0129626414410011](https://doi.org/10.1142/S0129626414410011)

BibTeX: [Download](#)

- Hannig F., Teich J.:

[**Proceedings of the First Workshop on Resource Awareness and Adaptivity in Multi-Core Computing \(Racing 2014\)**](#)

2014

BibTeX: [Download](#)

- Heisswolf J., Zaib A., Zwinkau A., Kobbe S., Weichslgartner A., Teich J., Henkel J., Snelling G., Herkersdorf A., Becker J.:

[**CAP: Communication Aware Programming**](#)

The 51st Annual Design Automation Conference (DAC) (San Francisco, CA, 2. Juni 2014 - 5. Juni 2014)

In: **Proc. of The 51st Annual Design Automation Conference (DAC)**, New York, NY, USA: 2014

DOI: [10.1145/2593069.2593103](https://doi.org/10.1145/2593069.2593103)

BibTeX: [Download](#)

- Herkersdorf A., Aliee H., Engel M., Glaß M., Gimmler-Dumont C., Henkel J., Kleeberger VB., Kochte MA., Kühn JM., Mueller-Gritschneider D., Nassif SR., Rauffuss H., Rosenstiel W., Schlichtmann U., Shafique M., Tahoori MB., Teich J., Wehn N., Weis C., Wunderlich HJ.:

[**Resilience Articulation Point \(RAP\): Cross-layer Dependability Modeling for Nanometer System-on-Chip Resilience**](#)

In: **Microelectronics Reliability** 54 (2014), p. 1066-1074

ISSN: 0026-2714

DOI: [10.1016/j.microrel.2013.12.012](https://doi.org/10.1016/j.microrel.2013.12.012)

BibTeX: [Download](#)

- Khosravi F., Reimann F., Glaß M., Teich J.:

[**Multi-objective local-search optimization using reliability importance measuring**](#)

51st Annual Design Automation Conference, DAC 2014 (San Francisco, CA, 1. Juni 2014 - 5. Juni 2014)

In: **Proceedings of the 51st Design Automation Conference (DAC 2014) 2014**

DOI: [10.1145/2593069.2593164](https://doi.org/10.1145/2593069.2593164)

BibTeX: [Download](#)

- Kuckuk S., Schmitt C., Köstler H., Hannig F., Teich J.:
[**Generating Highly Parallel Geometric Multigrid Solvers with the ExaStencils Approach**](#)
3rd Workshop on Extreme-scale Programming Tools (New Orleans, 17. November 2014 - 17. November 2014)
BibTeX: [Download](#)
- Lari V., Tanase AP., Hannig F., Teich J.:
[**Massively Parallel Processor Architectures for Resource-aware Computing**](#)
First Workshop on Resource Awareness and Adaptivity in Multi-Core Computing (Racing) (Paderborn, 29. Mai 2014 - 30. Mai 2014)
In: **Proc. of the First Workshop on Resource Awareness and Adaptivity in Multi-Core Computing (Racing 2014) 2014**
BibTeX: [Download](#)
- Lengauer C., Apel S., Bolten M., Größlinger A., Hannig F., Köstler H., Rude U., Teich J., Grebhahn A., Kronawitter S., Kuckuk S., Rittich H., Schmitt C.:
[**ExaStencils: Advanced Stencil-Code Engineering - First Project Report**](#)
(2014)
Open Access: <http://www.fim.uni-passau.de/fileadmin/files/forschung/mip-berichte/MIP1401.pdf>
BibTeX: [Download](#)
(Techreport)
- Lengauer C., Apel S., Größlinger A., Grebhahn A., Kronawitter S., Bolten M., Rittich H., Hannig F., Köstler H., Rude U., Teich J., Kuckuk S., Schmitt C.:
[**ExaStencils: Advanced Stencil-Code Engineering**](#)
Euro-Par: Parallel Processing Workshops (Porto, 25. August 2014 - 26. August 2014)
In: **Proceedings of Euro-Par 2014: Parallel Processing Workshops**, Berlin; Heidelberg: 2014
DOI: [10.1007/978-3-319-14313-2_47](https://doi.org/10.1007/978-3-319-14313-2_47)

URL: http://link.springer.com/content/pdf/10.1007/978-3-319-14313-2_47.pdf

BibTeX: [Download](#)

- Lukasiewicz M., Glaß M., Teich J., Chakraborty S.:
[Exploration of Distributed Automotive Systems using Compositional Timing Analysis](#)
In: **Embedded Systems Development: From Functional Models to Implementations**, Berlin; Heidelberg: Springer-Verlag, 2014, p. 189-204
ISBN: 978-1-4614-3878-6
BibTeX: [Download](#)
- Membarth R., Reiche O., Hannig F., Teich J.:
[Code Generation for Embedded Heterogeneous Architectures on Android](#)
Conference on Design, Automation and Test in Europe (DATE) (Dresden, 24. März 2014 - 28. März 2014)
In: **Proceedings of the Conference on Design, Automation and Test in Europe (DATE) 2014**
DOI: [10.7873/DATE2014.099](https://doi.org/10.7873/DATE2014.099)
BibTeX: [Download](#)
- Membarth R., Reiche O., Schmitt C., Hannig F., Teich J., Stürmer M., Köstler H.:
[Towards a Performance-portable Description of Geometric Multigrid Algorithms using a Domain-specific Language](#)
In: **Journal of Parallel and Distributed Computing** 74 (2014), p. 3191-3201
ISSN: 0743-7315
DOI: [10.1016/j.jpdc.2014.08.008](https://doi.org/10.1016/j.jpdc.2014.08.008)
BibTeX: [Download](#)
- Narayanan V., Teich J.:
[Introduction to the special issue on domain-specific multicore computing](#)
In: **Transactions on Embedded Computing Systems** 13 (2014), Article No.: 129
ISSN: 1558-3465
DOI: [10.1145/2588609](https://doi.org/10.1145/2588609)
BibTeX: [Download](#)
- Paul J., Stechele W., Sousa É., Lari V., Hannig F., Teich J., Kröhnert M., Asfour T.:

Self-Adaptive Harris Corner Detection on Heterogeneous Many-core Processor

2014 8th Conference on Design and Architectures for Signal and Image Processing, DASIP 2014 (Madrid, 8. Oktober 2014 - 10. Oktober 2014)

In: **Proc. of the Conference on Design and Architectures for Signal and Image Processing (DASIP)**, Gières, France: 2014

DOI: [10.1109/DASIP.2014.7115616](https://doi.org/10.1109/DASIP.2014.7115616)

BibTeX: [Download](#)

- Reiche O., Schmid M., Hannig F., Membarth R., Teich J.:

Code Generation from a Domain-specific Language for C-based HLS of Hardware Accelerators

International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) (New Dehli, 12. Oktober 2014 - 17. Oktober 2014)

In: **Proceedings of the International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)**, New York, NY, USA: 2014

DOI: [10.1145/2656075.2656081](https://doi.org/10.1145/2656075.2656081)

BibTeX: [Download](#)

- Reimann F., Glaß M., Teich J., Cook A., Gomez LR., Ull D., Wunderlich HJ., Engelke P., Abelein U.:

Advanced Diagnosis: SBST and BIST Integration in Automotive E/E Architectures

The 51st Annual Design Automation Conference (DAC) (San Francisco, CA, 2. Juni 2014 - 5. Juni 2014)

In: **Proc. of The 51st Annual Design Automation Conference (DAC)**, New York, NY, USA: 2014

DOI: [10.1145/2593069.2602971](https://doi.org/10.1145/2593069.2602971)

BibTeX: [Download](#)

- Roloff S., Hannig F., Teich J.:

Towards Actor-oriented Programming on PGAS-based Multicore Architectures

First International Workshop on Multi-Objective Many-Core Design (MOMAC) in conjunction with International Conference on Architecture of Computing Systems (ARCS) (Lübeck)

In: **Proc. of the first International Workshop on Multi-Objective Many-Core Design (MOMAC) in conjunction with International Conference on Architecture of Computing Systems (ARCS) 2014**

BibTeX: [Download](#)

- Rosales R., Glaß M., Teich J.:

[**Mahler: Sketch-based Model-driven Virtual Prototyping**](#)

In: **Proc. of the 27th International Conference on Architecture of Computing Systems (ARCS)**, New York, NY, USA: IEEE Press, 2014, p. 85-97 (Lecture Notes in Computer Science, Vol.8350)

ISBN: 978-3-319-04890-1

DOI: [10.1007/978-3-319-04891-8_8](https://doi.org/10.1007/978-3-319-04891-8_8)

BibTeX: [Download](#)

- Rosales R., Glaß M., Teich J., Wang B., Xu Y., Hasholzner R.:

[**MAESTRO - Holistic Actor-oriented Modeling of Non-Functional Properties and Firmware Behavior for MPSoCs**](#)

In: **ACM Transactions on Design Automation of Electronic Systems** 19 (2014), p. 23:1-23:26

ISSN: 1084-4309

DOI: [10.1145/2594481](https://doi.org/10.1145/2594481)

BibTeX: [Download](#)

- Schmid M., Apelt N., Hannig F., Teich J.:

[**An Image Processing Library for C-based High-Level Synthesis**](#)

Field-Programmable Logic and Applications (FPL) (Munich, 1. September 2014 - 5. September 2014)

In: **Proc. of Field-Programmable Logic and Applications (FPL)**, New York, NY, USA: 2014

DOI: [10.1109/FPL.2014.6927424](https://doi.org/10.1109/FPL.2014.6927424)

BibTeX: [Download](#)

- Schmid M., Hannig F., Tanase AP., Teich J.:

[**High-Level Synthesis Revised - Generation of FPGA Accelerators from a Domain-Specific Language using the Polyhedron Model**](#)

In: **Parallel Computing: Accelerating Computational Science and Enginee-**

ring (CSE), Amsterdam, The Netherlands: IOS Press, 2014, p. 497-506 (Advances in Parallel Computing, Vol.25)

ISBN: 978-1-61499-380-3

DOI: [10.3233/978-1-61499-381-0-497](https://doi.org/10.3233/978-1-61499-381-0-497)

BibTeX: [Download](#)

- Schmid M., Reiche O., Schmitt C., Hannig F., Teich J.:

[Code Generation for High-Level Synthesis of Multiresolution Applications on FPGAs](#)

First International Workshop on FPGAs for Software Programmers (FSP) (Munich, 1. September 2014 - 1. September 2014)

In: **Proc. of the First International Workshop on FPGAs for Software Programmers (FSP) 2014**

URL: <http://arxiv.org/abs/1408.4721>

BibTeX: [Download](#)

- Schmid M., Tanase AP., Hannig F., Teich J., Bhadouria VS., Ghoshal D.:

[Domain-Specific Augmentations for High-Level Synthesis](#)

25th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP) (Zurich, 18. Juni 2014 - 20. Juni 2014)

In: **Proc. of the 25th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)**, New York, NY, USA: 2014

DOI: [10.1109/ASAP.2014.6868653](https://doi.org/10.1109/ASAP.2014.6868653)

BibTeX: [Download](#)

- Schmidt B., Ziener D., Teich J.:

[An automatic netlist and floorplanning approach to improve the MTTR of scrubbing techniques](#)

2014 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, FPGA '14 (Monterey, CA, 26. Februar 2014 - 28. Februar 2014)

In: **In Proceedings of 2014 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, FPGA '14 2014**

BibTeX: [Download](#)

- Schmidt B., Ziener D., Teich J.:

[Minimizing Scrubbing Effort through Automatic Netlist Partitioning and Floorplanning](#)

Reconfigurable Architectures Workshop (RAW) (Phoenix, 19. Mai 2014 - 23. Mai 2014)

In: **Proc. of the Reconfigurable Architectures Workshop (RAW) 2014**

DOI: [10.1109/IPDPSW.2014.41](https://doi.org/10.1109/IPDPSW.2014.41)

BibTeX: [Download](#)

- Schmitt C., Kuckuk S., Hannig F., Köstler H., Teich J.:

[ExaSlang: A Domain-Specific Language for Highly Scalable Multigrid Solvers](#)

4th International Workshop on Domain-Specific Languages and High-Level Frameworks for High Performance Computing (WOLFHPC) (New Orleans, LA, USA, 17. November 2014 - 17. November 2014)

In: **Proc. of the 4th International Workshop on Domain-Specific Languages and High-Level Frameworks for High Performance Computing (WOLFHPC)**, New York, NY, USA: 2014

DOI: [10.1109/WOLFHPC.2014.11](https://doi.org/10.1109/WOLFHPC.2014.11)

BibTeX: [Download](#)

- Schmitt C., Kuckuk S., Köstler H., Hannig F., Teich J.:

[An Evaluation of Domain-Specific Language Technologies for Code Generation](#)

14th International Conference on Computational Science and its Applications (ICCSA) (Minho, Guimaraes, 30. Juni 2014 - 3. Juli 2014)

In: **Proc. of the 14th International Conference on Computational Science and its Applications (ICCSA)**, New York, NY, USA: 2014

DOI: [10.1109/ICCSA.2014.16](https://doi.org/10.1109/ICCSA.2014.16)

BibTeX: [Download](#)

- Seyler J., Rahimov S., Streichert T., Glaß M., Teich J.:

[DPSK modulated wakeup mechanism for point-to-point networks with partial network support](#)

9th IEEE International Symposium on Industrial Embedded Systems, SIES 2014 (Pisa)

In: **Proceedings of the 9th IEEE International Symposium on Industrial Embedded Systems (SIES) 2014**

DOI: [10.1109/SIES.2014.6871209](https://doi.org/10.1109/SIES.2014.6871209)

BibTeX: [Download](#)

- Seyler JR., Streichert T., Warkentin J., Spägle M., Glaß M., Teich J.:
[**A self-propagating wakeup mechanism for point-to-point networks with partial network support**](#)
17th Design, Automation and Test in Europe, DATE 2014 (Dresden, 24. März 2014 - 28. März 2014)
In: **Proceedings of Design, Automation and Test in Europe (DATE 2014)** 2014
DOI: [10.7873/DATE2014.019](https://doi.org/10.7873/DATE2014.019)
BibTeX: [Download](#)
- Sousa É., Gangadharan D., Hannig F., Teich J.:
[**Runtime reconfigurable bus arbitration for concurrent applications on heterogeneous MPSoC architectures**](#)
17th Euromicro Conference on Digital System Design, DSD 2014 (Verona, 27. August 2014 - 29. August 2014)
In: **Proceedings of the EUROMICRO Digital System Design Conference (DSD) 2014**
DOI: [10.1109/DSD.2014.105](https://doi.org/10.1109/DSD.2014.105)
BibTeX: [Download](#)
- Sousa É., Paul J., Lari V., Hannig F., Teich J., Stechele W.:
[**Resource-Aware Computer Vision Application on Heterogeneous Multi-Tile Architecture.**](#)
Hardware and Software Demo at the University Booth at Design, Automation and Test in Europe (DATE) (Dresden, 24. März 2014 - 28. Dezember 2017)
In: **Hardware and Software Demo at the University Booth at Design, Automation and Test in Europe (DATE) 2014**
Open Access: <https://www.date-conference.com/system/files/file/date14/ubooth/2615.pdf>
URL: <https://www.date-conference.com/system/files/file/date14/ubooth/2615.pdf>
BibTeX: [Download](#)
- Tanase AP., Witterauf M., Teich J., Hannig F.:
[**Symbolic inner loop parallelisation for massively parallel processor arrays**](#)

12th ACM/IEEE International Conference on Methods and Models for System Design, MEMOCODE 2014 (Lausanne, 19. Oktober 2014 - 21. Oktober 2014)

In: **Proceedings of the 12th ACM-IEEE International Conference on Formal Methods and Models for System Design (MEMOCODE) 2014**

DOI: [10.1109/MEMCOD.2014.6961865](https://doi.org/10.1109/MEMCOD.2014.6961865)

BibTeX: [Download](#)

- Teich J., Tanase AP., Hannig F.:

[Symbolic Mapping of Loop Programs onto Processor Arrays](#)

In: **Journal of Signal Processing Systems**, Berlin; Heidelberg: Springer-Verlag, 2014, p. 31-59

DOI: [10.1007/s11265-014-0905-0](https://doi.org/10.1007/s11265-014-0905-0)

BibTeX: [Download](#)

- Wang B., Xu Y., Rosales R., Hasholzner R., Glaß M., Teich J.:

[End-to-End Power Estimation for Heterogeneous Cellular LTE SoCs in Early Design Phases](#)

International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS) (Palma de Mallorca, 29. September 2014 - 1. Oktober 2014)

In: **Proceedings of the International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS) 2014**

DOI: [10.1109/PATMOS.2014.6951904](https://doi.org/10.1109/PATMOS.2014.6951904)

BibTeX: [Download](#)

- Weichslgartner A., Gangadharan D., Wildermann S., Glaß M., Teich J.:

[DAARM: Design-time application analysis and run-time mapping for predictable execution in many-core systems](#)

2014 International Conference on Hardware/Software Codesign and System Synthesis, CODES+ISSS 2014 (New Delhi, 12. Oktober 2014 - 17. Oktober 2014)

In: **Proceedings of the International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS 2014) 2014**

DOI: [10.1145/2656075.2656083](https://doi.org/10.1145/2656075.2656083)

BibTeX: [Download](#)

- Weichslgartner A., Teich J.:

[The Invasive Network on Chip - A Multi-Objective Many-Core Communication Infrastructure](#)

First International Workshop on Multi-Objective Many-Core Design (MOMAC) in conjunction with International Conference on Architecture of Computing Systems (ARCS) (Lübeck)

In: **Proc. of the first International Workshop on Multi-Objective Many-Core Design (MOMAC) in conjunction with International Conference on Architecture of Computing Systems (ARCS) 2014**

BibTeX: [Download](#)

- Wildermann S., Glaß M., Teich J.:
[**Multi-Objective Distributed Run-time Resource Management for Many-Cores**](#)
Design, Automation and Test in Europe (DATE) (Dresden, 24. März 2014 - 28. März 2014)
In: **Proc. of Design, Automation and Test in Europe (DATE)**, New York, NY, USA: 2014
DOI: [10.7873/DATE2014.234](https://doi.org/10.7873/DATE2014.234)
BibTeX: [Download](#)
- Wildermann S., Teich J.:
[**Self-Integration for Virtualization of Embedded Many-Core Systems**](#)
Workshop on Self-Improving System Integration (SISSY 2014) (London, 8. September 2014 - 8. September 2014)
In: **Proceedings of the Workshop on Self-Improving System Integration (SISSY 2014) 2014**
BibTeX: [Download](#)
- Xu Y., Wang B., Teich J.:
[**Parametric Yield Optimization Using Leakage-Yield-Driven Floorplanning**](#)
International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS) (Palma de Mallorca, 29. September 2014 - 1. Oktober 2014)
In: **Proceedings of the International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS) 2014**
DOI: [10.1109/PATMOS.2014.6951860](https://doi.org/10.1109/PATMOS.2014.6951860)
BibTeX: [Download](#)
- Zebelein C., Haubelt C., [Falk J.](#), Schwarzer T., Teich J.:
[**Model-based actor multiplexing with application to complex communication protocols**](#)

17th Design, Automation and Test in Europe, DATE 2014 (Dresden, 24. März 2014 - 28. März 2014)

In: **Proceedings of Design, Automation and Test in Europe (DATE 2014)**
2014

DOI: [10.7873/DATE2014.229](https://doi.org/10.7873/DATE2014.229)

BibTeX: [Download](#)

- Zhang L., [Falk J.](#), Schwarzer T., Glaß M., Teich J.:

[Communication-driven Automatic Virtual Prototyping for Networked Embedded Systems](#)

Euromicro Conference on Digital System Design (DSD) (Verona, 27. August 2014 - 29. August 2014)

In: **Proc. of Euromicro Conference on Digital System Design (DSD)**, New York, NY, USA: 2014

BibTeX: [Download](#)

2013

- Aliee H., Glaß M., Reimann F., Teich J.:

[Automatic Success Tree-Based Reliability Analysis for the Consideration of Transient and Permanent Faults](#)

Design, Automation and Test in Europe (DATE) (Grenoble, 18. März 2013 - 22. März 2013)

In: **Proc. Design, Automation and Test in Europe**, New York, NY, USA: 2013

DOI: [10.7873/DATE.2013.329](https://doi.org/10.7873/DATE.2013.329)

BibTeX: [Download](#)

- Boppu S., Hannig F., Teich J.:

[Loop Program Mapping and Compact Code Generation for Programmable Hardware Accelerators](#)

24th International Conference on Application-Specific Systems, Architectures and Processors (ASAP) (Washington, DC, 5. Juni 2013 - 7. Juni 2013)

In: **Proc. 24th International Conference on Application-Specific Systems, Architectures and Processors**, New York, NY, USA: 2013

DOI: [10.1109/ASAP.2013.6567544](https://doi.org/10.1109/ASAP.2013.6567544)

BibTeX: [Download](#)

- Boppu S., Lari V., Hannig F., Teich J.:
[Transactor-based Prototyping of Heterogeneous Multiprocessor System-On-Chip Architectures](#)
Synopsys Users Group Conference (SNUG) (Munich, 14. Mai 2013 - 14. Mai 2013)
In: **Proc. Synopsys Users Group Conference 2013**
BibTeX: [Download](#)
- Dennl C., Ziener D., Teich J.:
[Acceleration of SQL Restrictions and Aggregations through FPGA-based Dynamic Partial Reconfiguration](#)
IEEE International Field-Programmable Custom Computing Machines Symposium (FCCM) (Seattle, 28. April 2013 - 30. April 2013)
In: **Proc. IEEE International Field-Programmable Custom Computing Machines Symposium 2013**
DOI: [10.1109/FCCM.2013.38](#)
BibTeX: [Download](#)
- [Falk J.](#), Haubelt C., Teich J.:
[Integrated Modeling Using Finite State Machines and Dataflow Graphs](#)
In: huvra S. Bhattacharyya and Ed F. Deprettere and Rainer Leupers and Jarmo Takala (ed.): **Handbook of Signal Processing Systems**, 2013, p. 975-2013
DOI: [10.1007/978-1-4614-6859-2_30](#)
BibTeX: [Download](#)
- [Falk J.](#), Haubelt C., Zebelein C., Teich J.:
[Integrated Modeling Using Finite State Machines and Dataflow Graphs](#)
In: Bhattacharyya S., Deprettere E., Leupers R., Takala J. (ed.): **Handbook of Signal Processing Systems**, New York, NY: Springer, 2013
ISBN: 978-1-4614-6858-5
DOI: [10.1007/978-1-4614-6859-2_30](#)
BibTeX: [Download](#)
- [Falk J.](#), Zebelein C., Haubelt C., Teich J.:
[A Rule-Based Quasi-Static Scheduling Approach for Static Islands in Dynamic Dataflow Graphs](#)
In: **ACM Transactions on Embedded Computing Systems**, New York, NY:

ACM, 2013, p. 74:1-74:31

DOI: [10.1145/2442116.2442124](https://doi.org/10.1145/2442116.2442124)

BibTeX: [Download](#)

- [Falk J.](#), Zebelein C., Haubelt C., Teich J.:

[A rule-based quasi-static scheduling approach for static islands in dynamic dataflow graphs](#)

In: **ACM Transactions on Embedded Computing Systems** 12 (2013), Article No.: 74

ISSN: 1539-9087

DOI: [10.1145/2442116.2442124](https://doi.org/10.1145/2442116.2442124)

BibTeX: [Download](#)

- Glock S., Rosales R., Reutelhuber F., Glaß M., Teich J., Fischer G., Weigel R., Ußmüller T.:

[Scenario-Based Energy Estimation of Heterogeneous Integrated Systems at System Level](#)

43rd European Microwave Conference (EuMC) (Nuremberg, 7. Oktober 2013 - 10. Oktober 2013)

In: **Proc. 43rd European Microwave Conference 2013**

BibTeX: [Download](#)

- Graf S., Glaß M., Teich J.:

[Investigating the Impact of Energy-Efficient Ethernet on Automotive Applications via High-level Modeling](#)

Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV) (Warnemünde, 12. März 2013 - 14. März 2013)

In: **Tagungsunterlagen Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen**, Rostock: 2013

BibTeX: [Download](#)

- Graf S., Glaß M., Wintermann D., Teich J., Lauer C.:

[IVaM: Implicit Variant Modeling and Management for Automotive Embedded Systems](#)

International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) (Montreal, QC, 29. September 2013 - 4. Oktober 2013)

In: **Proc. International Conference on Hardware/Software Codesign and System Synthesis**, New York, NY, USA: 2013

DOI: [10.1109/CODES-ISSS.2013.6658982](https://doi.org/10.1109/CODES-ISSS.2013.6658982)

BibTeX: [Download](#)

- Hannig F., Schmid M., Lari V., Boppu S., Teich J.:

[**System Integration of Tightly-Coupled Processor Arrays using Reconfigurable Buffer Structures**](#)

ACM International Conference on Computing Frontiers (CF) (Ischia, 14. Mai 2013 - 16. Mai 2013)

In: **Proc. ACM International Conference on Computing Frontiers**, New York, NY, USA: 2013

DOI: [10.1145/2482767.2482770](https://doi.org/10.1145/2482767.2482770)

BibTeX: [Download](#)

- Heisswolf J., Weichslgartner A., Zaib A., König R., Wild T., Herkersdorf A., Teich J., Becker J.:

[**Hardware Supported Adaptive Data Collection for Networks on Chip**](#)

IEEE 27th International Parallel and Distributed Processing Symposium Workshops PhD Forum (IPDPSW) (Boston, Massachusetts, 20. Mai 2013 - 24. Mai 2013)

In: **Proc. IEEE 27th International Parallel and Distributed Processing Symposium Workshops PhD Forum**, Red Hook, NY, USA: 2013

DOI: [10.1109/IPDPSW.2013.124](https://doi.org/10.1109/IPDPSW.2013.124)

BibTeX: [Download](#)

- Heisswolf J., Zaib A., Weichslgartner A., König R., Wild T., Teich J., Herkersdorf A., Becker J.:

[**Virtual Networks - Distributed Communication Resource Management**](#)

In: **ACM Transactions on Reconfigurable Technology and Systems** 6 (2013), p. 8:1-8:14

ISSN: 1936-7406

DOI: [10.1145/2492186](https://doi.org/10.1145/2492186)

BibTeX: [Download](#)

- Henkel J., Narayanan V., Parameswaran S., Teich J.:

[**Run-time adaption for highly-complex multi-core systems**](#)

11th ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis, CODES+ISSS 2013 (Montreal, QC, 29. September 2013 - 4. Oktober 2013)

DOI: [10.1109/CODES-ISSS.2013.6659000](https://doi.org/10.1109/CODES-ISSS.2013.6659000)

BibTeX: [Download](#)

- Herkersdorf A., Engel M., Glaß M., Henkel J., Kleeberger VB., Kochte MA., Kühn JM., Nassif SR., Rauchfuss H., Rosenstiel W., Schlichtmann U., Shafique M., Tahoori MB., Teich J., Wehn N., Weis C., Wunderlich HJ.:

[Cross-Layer Dependability Modeling and Abstraction in System on Chip](#)

9th Workshop on Silicon Errors in Logic - System Effects (SELSE) (Palo Alto, CA, 26. März 2013 - 27. März 2013)

In: **Proc. 9th Workshop on Silicon Errors in Logic - System Effects**, München: 2013

URL: <http://www.selse.org>

BibTeX: [Download](#)

- Mostaghim S., Teich J.:

[Strategies for finding good local guides in multi-objective particle swarm optimization \(MOPSO\)](#)

2003 IEEE Swarm Intelligence Symposium, SIS 2003

DOI: [10.1109/SIS.2003.1202243](https://doi.org/10.1109/SIS.2003.1202243)

BibTeX: [Download](#)

- Reimann F., Glaß M., Teich J.:

[Migration Strategies for Ethernet-based E/E Architectures](#)

Embedded World Conference (Nuremberg, 26. Februar 2013 - 28. Februar 2013)

In: **Proc. Embedded World Conference**, Nuremberg, Germany: 2013

BibTeX: [Download](#)

- Reimann F., Glaß M., Teich J., Abelein U.:

[Szenarienbasierte Integration von Diagnosefunktionalität in E/E Architekturen](#)

Automotive meets Electronics (AmE) (Dortmund, 19. Februar 2013 - 20. Februar 2013)

- In: **Proc. Automotive meets Electronics, GMM Fachbericht 75**, Berlin, Germany: 2013
BibTeX: [Download](#)
- Reimann F., Graf S., Streit F., Glaß M., Teich J.:
[Timing Analysis of Ethernet AVB-based Automotive E/E Architectures](#)
IEEE International Conference on Emerging Technology & Factory Automation (ETFA) (Cagliari, 10. September 2013 - 13. September 2013)
In: **Proc. IEEE International Conference on Emerging Technology & Factory Automation**, Red Hook, NY, USA: 2013
DOI: [10.1109/ETFA.2013.6648024](https://doi.org/10.1109/ETFA.2013.6648024)
URL: <http://www.etfa2013.org>
BibTeX: [Download](#)
 - Roloff S., Weichslgartner A., Heißwolf J., Hannig F., Teich J.:
[NoC Simulation in Heterogeneous Architectures for PGAS Programming Model](#)
16th International Workshop on Software and Compilers for Embedded Systems (M-SCOPES) (St. Goar, 19. Juni 2013 - 21. Juni 2013)
In: **Proc. 16th International Workshop on Software and Compilers for Embedded Systems**, New York, NY, USA: 2013
DOI: [10.1145/2463596.2463606](https://doi.org/10.1145/2463596.2463606)
BibTeX: [Download](#)
 - Schmid M., Blocherer M., Hannig F., Teich J.:
[Real-Time Range Image Preprocessing on FPGAs](#)
International Conference on Reconfigurable Computing and FPGAs (ReConFig) (Cancun, 9. Dezember 2013 - 11. Dezember 2013)
In: **Proc. International Conference on Reconfigurable Computing and FPGAs 2013**
DOI: [10.1109/ReConFig.2013.6732325](https://doi.org/10.1109/ReConFig.2013.6732325)
BibTeX: [Download](#)
 - Sousa É., Tanase AP., Hannig F., Teich J.:
[Accuracy and Performance Analysis of Harris Corner Computation on Tightly-Coupled Processor Arrays](#)
2013 Conference on Design and Architectures for Signal and Image Processing

(DASIP) (Cagliari, 8. Oktober 2013 - 10. Oktober 2013)

In: **Proc. 2013 Conference on Design and Architectures for Signal and Image Processing**, New York, NY, USA: 2013

BibTeX: [Download](#)

- Sousa É., Tanase AP., Hannig F., Teich J.:

[A Prototype of an Adaptive Computer Vision Algorithm on MPSoC Architecture](#)

2013 Conference on Design and Architectures for Signal and Image Processing (DASIP) (Cagliari, 8. Oktober 2013 - 10. Oktober 2013)

In: **Proc. 2013 Conference on Design and Architectures for Signal and Image Processing**, New York, NY, USA: 2013

BibTeX: [Download](#)

- Sousa É., Tanase AP., Lari V., Hannig F., Teich J., Paul J., Stechele W., Kröhnert M., Asfour T.:

[Acceleration of Optical Flow Computations on Tightly-Coupled Processor Arrays](#)

25th Workshop on Parallel Systems and Algorithms (PARS) (Erlangen)

In: **Proc. 25th Workshop on Parallel Systems and Algorithms**, Berlin, Germany: 2013

BibTeX: [Download](#)

- Tanase AP., Lari V., Hannig F., Teich J.:

[Exploitation of Quality/Throughput Tradeoffs in Image Processing through Invasive Computing](#)

International Conference on Parallel Computing (ParCo) (Munich, 10. September 2013 - 13. September 2013)

In: **Proc. International Conference on Parallel Computing 2013**

BibTeX: [Download](#)

- Teich J., Schröder-Preikschat W., Herkersdorf A.:

[Invasive Computing - Common Terms and Granularity of Invasion](#)

Cornell: Cornell University Library, 2013

(Dagstuhl Preprint Serie)

URL: <http://arxiv.org/pdf/1304.6067v1.pdf>

BibTeX: [Download](#)

- Teich J., Tanase AP., Hannig F.:
[Symbolic Parallelization of Loop Programs for Massively Parallel Processor Arrays](#)
24th International Conference on Application-Specific Systems, Architectures and Processors (ASAP) (Washington, DC, 5. Juni 2013 - 7. Juni 2013)
In: **Proc. 24th International Conference on Application-Specific Systems, Architectures and Processors**, New York, NY, USA: 2013
DOI: [10.1109/ASAP.2013.6567543](https://doi.org/10.1109/ASAP.2013.6567543)
BibTeX: [Download](#)
- Wildermann S., Teich J.:
[Decomposing Run-time Resource Management in Heterogeneous Reconfigurable Systems](#)
Workshop on Self-Awareness in Reconfigurable Computing Systems (SRCS) (Porto)
In: **Proc. Workshop on Self-Awareness in Reconfigurable Computing Systems** 2013
BibTeX: [Download](#)
- Wildermann S., Ziermann T., Teich J.:
[Game-Theoretic Analysis of Decentralized Core Allocation Schemes on Many-core Systems](#)
Design, Automation and Test in Europe (DATE) (Grenoble, 18. März 2013 - 22. März 2013)
In: **Proc. Design, Automation and Test in Europe**, New York, NY, USA: 2013
DOI: [10.7873/DATE.2013.305](https://doi.org/10.7873/DATE.2013.305)
BibTeX: [Download](#)
- Xu Y., Wang B., Hasholzner R., Rosales R., Teich J.:
[On robust task-accurate performance estimation](#)
50th Annual Design Automation Conference, DAC 2013 (Austin, TX, 2. Juni 2013 - 6. Juni 2013)
In: **Proceedings of the 50th Design Automation Conference (DAC 2013)** 2013
DOI: [10.1145/2463209.2488945](https://doi.org/10.1145/2463209.2488945)
BibTeX: [Download](#)

- Xu Y., Wang B., Rosales R., Hasholzner R., Teich J.:
[On confident task-accurate performance estimation](#)
26th International Conference on Architecture of Computing Systems, ARCS 2013 (Prague)
In: **Proceedings of the International Conference on Architecture of Computing Systems (ARCS) 2013**
DOI: [10.1007/978-3-642-36424-2_3](https://doi.org/10.1007/978-3-642-36424-2_3)
BibTeX: [Download](#)
- Zaib A., Heisswolf J., Weichslgartner A., Wild T., Teich J., Becker J., Herkersdorf A.:
[AUTO-GS: Self-optimization of NoC Traffic Through Hardware Managed Virtual Connections](#)
16th Euromicro Conference on Digital System Design (Cantabria, 4. September 2013 - 6. September 2013)
In: **Proc. 16th Euromicro Conference on Digital System Design 2013**
DOI: [10.1109/DSD.2013.87](https://doi.org/10.1109/DSD.2013.87)
BibTeX: [Download](#)
- Zebelein C., Haubelt C., [Falk J.](#), Schwarzer T., Teich J.:
[Representing mapping and scheduling decisions within dataflow graphs](#)
2013 16th Forum on Specification and Design Languages, FDL 2013 (Paris, 24. September 2013 - 26. September 2013)
In: **Proceedings of Forum on Specification & Design Languages (FDL 2013) 2013**
URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=84891286674&origin=inward>
BibTeX: [Download](#)
- Zebelein C., Haubelt C., [Falk J.](#), Teich J.:
[Model-Based Representation of Schedules for Dataflow Graphs](#)
Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV 2013) (Rostock, 12. März 2013 - 14. März 2013)
In: **Proceedings of Methoden und Beschreibungssprachen zur Modellierung**

und Verifikation von Schaltungen und Systemen (MBMV 2013) 2013

BibTeX: [Download](#)

- Zhang L., Glaß M., Ballmann N., Teich J.:
[**Bridging Algorithm and ESL Design: Matlab/Simulink Model Transformation and Validation**](#)
Forum on Specification & Design Languages (FDL) (Paris, 24. September 2013 - 26. September 2013)
In: **Proc. Forum on Specification & Design Languages**, New York, NY, USA: 2013
BibTeX: [Download](#)
- Ziermann T., Salcic Z., Teich J.:
[**HW/SW Tradeoffs for Dynamic Message Scheduling in Controller Area Network \(CAN\)**](#)
26th International Conference on Architecture of Computing Systems (ARCS) (Prague, 19. Februar 2013 - 22. Februar 2013)
In: **Proc. 26th International Conference on Architecture of Computing Systems**, New York, NY, USA: 2013
DOI: [10.1007/978-3-642-36424-2_14](#)
BibTeX: [Download](#)
- Ziermann T., Wildermann S., Teich J.:
[**Self-organizing Core Allocation**](#)
Parallel-Algorithmen, -Rechnerstrukturen und -Systemsoftware (PARS) (Erlangen, 11. April 2013 - 12. April 2013)
In: **Proc. Parallel-Algorithmen, -Rechnerstrukturen und -Systemsoftware** 2013
BibTeX: [Download](#)

2012

- Dennl C., Ziener D., Teich J.:
[**On-the-fly Composition of FPGA-Based SQL Query Accelerators Using A Partially Reconfigurable Module Library**](#)
IEEE International Field-Programmable Custom Computing Machines Symposium (FCCM) (Toronto, 29. April 2012 - 1. Mai 2012)

In: **Proc. of the IEEE International Field-Programmable Custom Computing Machines Symposium (FCCM)**, New York, NY, USA: 2012

DOI: [10.1109/FCCM.2012.18](https://doi.org/10.1109/FCCM.2012.18)

BibTeX: [Download](#)

- Eberl M., Glaß M., Teich J., Abelein U.:

[Considering Diagnosis Functionality during Automatic System-Level Design of Automotive Networks](#)

The 49th Annual Design Automation Conference 2012 (DAC) (San Francisco, CA, 3. Juni 2012 - 7. Juni 2012)

In: **Proc. of The 49th Annual Design Automation Conference 2012 (DAC)**, New York, NY, USA: 2012

DOI: [10.1145/2228360.2228400](https://doi.org/10.1145/2228360.2228400)

BibTeX: [Download](#)

- Fekete SP., Kamphans T., Schweer N., Tessars C., Van Der Veen JC., Angermeyer J., Koch D., Teich J.:

[Dynamic Defragmentation of Reconfigurable Devices](#)

In: **ACM Transactions on Reconfigurable Technology and Systems** 5 (2012), p. 1-20

ISSN: 1936-7406

DOI: [10.1145/2209285.2209287](https://doi.org/10.1145/2209285.2209287)

BibTeX: [Download](#)

- Gladigau J., Haubelt C., Teich J.:

[Model-Based Virtual Prototype Acceleration](#)

In: **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems** 31 (2012), p. 1572-1585

ISSN: 0278-0070

DOI: [10.1109/TCAD.2012.2205148](https://doi.org/10.1109/TCAD.2012.2205148)

BibTeX: [Download](#)

- Glaß M., Teich J., Zhang L.:

[A Co-simulation Approach for System-Level Analysis of Embedded Control Systems](#)

2012 International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS) (Samos, 16. Juli 2012 - 19. Juli 2012)

In: **Proc. of the 2012 International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS)**, New York, NY, USA: 2012

DOI: [10.1109/SAMOS.2012.6404200](https://doi.org/10.1109/SAMOS.2012.6404200)

BibTeX: [Download](#)

- Glaß M., Yu H., Reimann F., Teich J.:
[**Cross-Level Compositional Reliability Analysis for Embedded Systems**](#)
31st International Conference on Computer Safety, Reliability, and Security (SAFECOMP) (Magdeburg, 25. September 2012 - 28. September 2012)
In: **Proc. of the 31st International Conference on Computer Safety, Reliability, and Security (SAFECOMP)**, Berlin; Heidelberg: 2012
DOI: [10.1007/978-3-642-33678-2_10](https://doi.org/10.1007/978-3-642-33678-2_10)
BibTeX: [Download](#)
- Graf S., Glaß M., Teich J.:
[**Unreliable Data Transmissions and Limited Hardware Communication Buffers in Automotive E/E Virtual Prototypes**](#)
Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV) (Kaiserslautern, 5. März 2012 - 7. März 2012)
In: **Tagungsunterlagen Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV)**, Hamburg, Germany: 2012
BibTeX: [Download](#)
- Graf S., Russ T., Glaß M., Teich J.:
[**Considering MOST150 during Virtual Prototyping of Automotive E/E Architectures**](#)
Automotive meets Electronics (AmE), GMM Fachbericht 72 (Dortmund)
In: **Proc. of Automotive meets Electronics (AmE), GMM Fachbericht 72**, Berlin, Germany: 2012
BibTeX: [Download](#)
- Heisswolf J., Zaib A., Weichslgartner A., König R., Wild T., Teich J., Herkersdorf A., Becker J.:
[**Hardware-assisted Decentralized Resource Management for Networks on**](#)

Chip with QoS

26th IEEE International Parallel and Distributed Processing Symposium Workshops & PhD Forum (IPDPSW) (Shanghai, 21. Mai 2012 - 25. Mai 2012)

In: **Proc. of the 26th IEEE International Parallel and Distributed Processing Symposium Workshops & PhD Forum (IPDPSW)**, New York, NY, USA: 2012

DOI: [10.1109/IPDPSW.2012.25](https://doi.org/10.1109/IPDPSW.2012.25)

BibTeX: [Download](#)

- Kiesel R., Streubühr M., Haubelt C., Terzis A., Teich J.:

Virtual prototyping for efficient multi-core ECU development of driver assistance systems

2012 International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation, IC-SAMOS 2012 (Samos, 16. Juli 2012 - 19. Juli 2012)

In: **Proceedings of the International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS XII) 2012**

DOI: [10.1109/SAMOS.2012.6404155](https://doi.org/10.1109/SAMOS.2012.6404155)

BibTeX: [Download](#)

- Koch D., Torresen J., Beckhoff C., Ziener D., Dennl C., Breuer V., Teich J., Feilen M., Stechele W.:

Partial Reconfiguration on FPGAs in Practice - Tools and Applications

25th International Conference on Architecture of Computing Systems (ARCS) (Munich, 28. Februar 2012 - 2. März 2012)

In: **Proc. of the 25th International Conference on Architecture of Computing Systems (ARCS)**, New York, NY, USA: 2012

BibTeX: [Download](#)

- Lari V., Muddasani S., Boppu S., Hannig F., Schmid M., Teich J.:

Hierarchical Power Management for Adaptive Tightly-Coupled Processor Arrays

In: **ACM Transactions on Design Automation of Electronic Systems** 18 (2012), p. 1-25

ISSN: 1084-4309

DOI: [10.1145/2390191.2390193](https://doi.org/10.1145/2390191.2390193)

BibTeX: [Download](#)

- Lari V., Muddasani S., Boppu S., Hannig F., Teich J.:
[Design of low power on-chip processor arrays](#)
2012 IEEE 23rd International Conference on Application-Specific Systems, Architectures and Processors, ASAP 2012 (Delft, 9. Juli 2012 - 11. Juli 2012)
In: **Proceedings of the 23rd IEEE International Conference on Application-specific Systems, Architectures, and Processors (ASAP) 2012**
DOI: [10.1109/ASAP.2012.10](https://doi.org/10.1109/ASAP.2012.10)
BibTeX: [Download](#)
- Lukasiwycz M., Glaß M., Teich J., Milbredt P.:
[FlexRay Static Segment Scheduling](#)
In: **Advances in Real-Time Systems**, Berlin; Heidelberg: Springer-Verlag, 2012, p. 323-339
ISBN: 978-3-642-24348-6
BibTeX: [Download](#)
- Membarth R., Hannig F., Teich J., Körner M., Eckert W.:
[Automatic Optimization of In-Flight Memory Transactions for GPU Accelerators based on a Domain-Specific Language for Medical Imaging](#)
11th International Symposium on Parallel and Distributed Computing (ISPDC) (Munich, 25. Juni 2012 - 29. Juni 2012)
In: **Proc. of the 11th International Symposium on Parallel and Distributed Computing (ISPDC)**, New York, NY, USA: 2012
DOI: [10.1109/ISPDC.2012.36](https://doi.org/10.1109/ISPDC.2012.36)
BibTeX: [Download](#)
- Membarth R., Hannig F., Teich J., Körner M., Eckert W.:
[Generating Device-specific GPU Code for Local Operators in Medical Imaging](#)
26th IEEE International Parallel and Distributed Processing Symposium (IPDPS) (Shanghai, 21. Mai 2012 - 25. Mai 2012)
In: **Proc. of the 26th IEEE International Parallel and Distributed Processing Symposium (IPDPS)**, New York, NY, USA: 2012
DOI: [10.1109/IPDPS.2012.59](https://doi.org/10.1109/IPDPS.2012.59)
BibTeX: [Download](#)

- Membarth R., Hannig F., Teich J., Körner M., Eckert W.:
[Mastering Software Variant Explosion for GPU Accelerators](#)
In: **Proceedings of the 10th International Workshop on Algorithms, Models and Tools for Parallel Computing on Heterogeneous Platforms (HeteroPar)**, Berlin; Heidelberg: Springer, 2012, p. 123-132 (Lecture Notes on Computer Science (LNCS))
DOI: [10.1007/978-3-642-36949-0_15](https://doi.org/10.1007/978-3-642-36949-0_15)
BibTeX: [Download](#)
- Membarth R., Hannig F., Teich J., Köstler H.:
[Towards Domain-specific Computing for Stencil Codes in HPC](#)
2nd International Workshop on Domain-Specific Languages and High-Level Frameworks for High Performance Computing (WOLFHPC) (Salt Lake City, UT, 10. November 2012 - 16. November 2012)
In: **Proceedings of the 2nd International Workshop on Domain-Specific Languages and High-Level Frameworks for High Performance Computing (WOLFHPC) 2012**
DOI: [10.1109/SC.Companion.2012.136](https://doi.org/10.1109/SC.Companion.2012.136)
BibTeX: [Download](#)
- Membarth R., Lupp JH., Hannig F., Teich J., Körner M., Eckert W.:
[Dynamic Task-Scheduling and Resource Management for GPU Accelerators in Medical Imaging](#)
25th International Conference on Architecture of Computing Systems (ARCS) (Munich, 28. Februar 2012 - 2. März 2012)
In: **Proc. of the 25th International Conference on Architecture of Computing Systems (ARCS)**, New York, NY, USA: 2012
DOI: [10.1007/978-3-642-28293-5_13](https://doi.org/10.1007/978-3-642-28293-5_13)
BibTeX: [Download](#)
- Milbredt P., Glaß M., Lukasiewicz M., Steininger A., Teich J.:
[Designing FlexRay-based Automotive Architectures: A Holistic OEM Approach](#)
Design, Automation and Test in Europe (DATE) (Dresden, Germany, 12. März 2012 - 16. März 2012)
In: **Proc. of Design, Automation and Test in Europe (DATE)**, New York, NY,

USA: 2012

BibTeX: [Download](#)

- Muddasani S., Boppu S., Hannig F., Kuzmin B., Lari V., Teich J.:
[A Prototype of an Invasive Tightly-Coupled Processor Array](#)
2012 Conference on Design and Architectures for Signal and Image Processing (DASIP) (Karlsruhe, 23. Oktober 2012 - 25. Oktober 2012)
In: **Proc. of the 2012 Conference on Design and Architectures for Signal and Image Processing (DASIP)**, New York, NY, USA: 2012
BibTeX: [Download](#)
- Roloff S., Hannig F., Teich J.:
[Approximate Time Functional Simulation of Resource-Aware Programming Concepts for Heterogeneous MPSoCs](#)
17th Asia and South Pacific Design Automation Conference (ASP-DAC) (Sydney, 30. Januar 2012 - 2. Februar 2012)
In: **Proc. of the 17th Asia and South Pacific Design Automation Conference (ASP-DAC)**, New York, NY, USA: 2012
DOI: [10.1109/ASPDAC.2012.6164943](https://doi.org/10.1109/ASPDAC.2012.6164943)
BibTeX: [Download](#)
- Roloff S., Hannig F., Teich J.:
[Fast Architecture Evaluation of Heterogeneous MPSoCs by Host-Compiled Simulation](#)
15th International Workshop on Software and Compilers for Embedded Systems (SCOPES) (Schloss Rheinfels, St. Goar, 15. Mai 2012 - 16. Mai 2012)
In: **Proc. of the 15th International Workshop on Software and Compilers for Embedded Systems (SCOPES)**, New York, NY, USA: 2012
DOI: [10.1145/2236576.2236582](https://doi.org/10.1145/2236576.2236582)
BibTeX: [Download](#)
- Roloff S., Hannig F., Teich J.:
[Simulation of Resource-Aware Applications on Heterogeneous Architectures](#)
8th International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems (ACACES) (Fiuggi, 8. Juli 2012 - 14. Juli 2012)

In: **Proc. of the 8th International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems (ACACES)**, Ghent, Belgium: 2012

BibTeX: [Download](#)

- Rosales R., Klie T., Glock S., Xu Y., Wang B., Hasholzner R., Teich J., Weigel R.:

[**Eine Aktor-Orientierte Methodik zur Power-Modellierung auf Systemebene**](#)

In: **Design & Elektronik** (2012), p. 1-9

ISSN: 0933-8667

BibTeX: [Download](#)

- Schmid M., Hannig F., Teich J.:

[**Power Management Strategies for Serial RapidIO Endpoints in FPGAs**](#)

IEEE International Field-Programmable Custom Computing Machines Symposium (FCCM) (Toronto, 29. April 2012 - 1. Mai 2012)

In: **Proc. of the IEEE International Field-Programmable Custom Computing Machines Symposium (FCCM)**, New York, NY, USA: 2012

DOI: [10.1109/FCCM.2012.26](https://doi.org/10.1109/FCCM.2012.26)

BibTeX: [Download](#)

- Tanase AP., Hannig F., Teich J.:

[**Symbolic loop parallelization of static control programs**](#)

8th International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems (ACACES) (Fiuggi, 8. Juli 2012 - 14. Juli 2012)

In: **Proc. of the 8th International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems (ACACES)**, Ghent, Belgium: 2012

BibTeX: [Download](#)

- Teich J.:

[**Hardware/Software Co-Design: Past, Present, and Predicting the Future**](#)

In: **Proceedings of the IEEE 100** (2012), p. 1411-1430

ISSN: 0018-9219

DOI: [10.1109/JPROC.2011.2182009](https://doi.org/10.1109/JPROC.2011.2182009)

BibTeX: [Download](#)

- Teich J., Weichslgartner A., Oechslein B., Schröder-Preikschat W.:
[Invasive Computing - Concepts and Overheads](#)
Forum on Specification & Design Languages (FDL) (Vienna, 18. September 2012 - 20. September 2012)
In: **Proc. of the Forum on Specification & Design Languages (FDL)**, New York, NY, USA: 2012
BibTeX: [Download](#)
- Wildermann S., Angermeier J., Sibirko E., Teich J.:
[Placing Multi-mode Streaming Applications on Dynamically Partially Reconfigurable Architectures](#)
In: **International Journal of Reconfigurable Computing** 2012 (2012), p. 1-12
ISSN: 1687-7195
DOI: [10.1155/2012/608312](#)
BibTeX: [Download](#)
- Wildermann S., Reimann F., Ziener D., Teich J.:
[Symbolic System-level Design Methodology for Multi-Mode Reconfigurable Systems](#)
In: **Design Automation For Embedded Systems** (2012), p. 1-33
ISSN: 0929-5585
DOI: [10.1007/s10617-012-9102-1](#)
BibTeX: [Download](#)
- Wildermann S., Reimann F., Ziener D., Teich J.:
[System Level Synthesis Flow for Self-adaptive Multi-mode Reconfigurable Systems](#)
Workshop on Self-Awareness in Reconfigurable Computing Systems (SRCS) (Oslo, 1. September 2012 - 1. September 2012)
In: **Proc. of the Workshop on Self-Awareness in Reconfigurable Computing Systems (SRCS) 2012**
BibTeX: [Download](#)
- Xu Y., Rosales R., Wang B., Streubühr M., Hasholzner R., Haubelt C., Teich J.:
[A very fast and quasi-accurate power-state-based system-level power modeling methodology](#)
25th International Conference on Architecture of Computing Systems, ARCS

2012 (Munich)

In: **Proceedings of the International Conference on Architecture of Computing Systems (ARCS) 2012**

DOI: [10.1007/978-3-642-28293-5_4](https://doi.org/10.1007/978-3-642-28293-5_4)

BibTeX: [Download](#)

- Zebelein C., [Falk J.](#), Haubelt C., Teich J.:

[A model-based inter-process resource sharing approach for high-level synthesis of dataflow graphs](#)

2nd Electronic System Level Synthesis Conference, ESLsyn 2012 (San Francisco, CA, 2. Juni 2012 - 3. Juni 2012)

URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=84866155902&origin=inward>

BibTeX: [Download](#)

- Zebelein C., [Falk J.](#), Haubelt C., Teich J.:

[Exploiting Model-Knowledge in High-Level Synthesis](#)

Workshop für Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV'12) (Kaiserslautern, 5. März 2012 - 7. März 2012)

In: **Workshop für Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV'12) 2012**

BibTeX: [Download](#)

- Zhang L., Glaß M., Streubühr M., Teich J., von Schwerin A., Liu K.:

[Actor-oriented Modeling and Simulation of Cut-through Communication in Network Controllers](#)

Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV) (Kaiserslautern, 5. März 2012 - 7. März 2012)

In: **Tagungsunterlagen Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV)**, Hamburg, Germany: 2012

BibTeX: [Download](#)

- Zhang L., Streubühr M., Glaß M., Teich J., von Schwerin A., Liu K.:
[System-Level Modeling and Simulation of Networked PROFINET IO Controllers](#)
Embedded World Conference (Nuremberg, 28. Februar 2012 - 1. März 2013)
In: **Proc. of the Embedded World Conference**, Kissingen, Germany: 2012
BibTeX: [Download](#)
- Ziermann T., Butiu A., Teich J., Ziener D.:
[FPGA-based Testbed for Timing Behavior Evaluation of the Controller Area Network \(CAN\)](#)
2012 International Conference on Reconfigurable Computing (ReConFig) (Cancun, 5. Dezember 2012 - 7. Dezember 2012)
In: **Proc. of the 2012 International Conference on Reconfigurable Computing (ReConFig)**, New York, NY, USA: 2012
DOI: [10.1109/ReConFig.2012.6416750](https://doi.org/10.1109/ReConFig.2012.6416750)
BibTeX: [Download](#)
- Ziermann T., Salcic Z., Teich J.:
[Improving Performance of Controller Area Network \(CAN\) by Adaptive Message Scheduling](#)
In: **Self-Organization in Embedded Real-Time Systems**, Berlin; Heidelberg: Springer-Verlag, 2012, p. 95-120
ISBN: 978-1-4614-1968-6
BibTeX: [Download](#)
- Ziermann T., Wildermann S., Mühleis N., Teich J.:
[Distributed self-organizing bandwidth allocation for priority-based bus communication](#)
In: **Concurrency and Computation-Practice & Experience** 24 (2012), p. 1903-1917
ISSN: 1532-0626
DOI: [10.1002/cpe.1759](https://doi.org/10.1002/cpe.1759)
BibTeX: [Download](#)

2011

- Angermeier J., Sibirko E., [Wanka R.](#), Teich J.:
[**Bitonic Sorting on Dynamically Reconfigurable Architectures**](#)
IEEE International Symposium on Parallel and Distributed Processing Workshops and Phd Forum (IPDPSW) (Anchorage, AL, 16. Mai 2011 - 20. Mai 2011)
In: **Proc. IEEE International Symposium on Parallel and Distributed Processing Workshops and Phd Forum (IPDPSW)**, New York, NY, USA: 2011
DOI: [10.1109/IPDPS.2011.164](https://doi.org/10.1109/IPDPS.2011.164)
BibTeX: [Download](#)
- Angermeier J., Ziener D., Glaß M., Teich J.:
[**Runtime Stress-Aware Replica Placement on Reconfigurable Devices under Safety Constraints**](#)
International Conference on Field-Programmable Technology (FPT'11) (New Delhi, 12. Dezember 2011 - 14. Dezember 2011)
In: **Proceedings of the International Conference on Field-Programmable Technology**, New York, NY, USA: 2011
DOI: [10.1109/FPT.2011.6133247](https://doi.org/10.1109/FPT.2011.6133247)
BibTeX: [Download](#)
- Angermeier J., Ziener D., Glaß M., Teich J.:
[**Stress-Aware Module Placement on Reconfigurable Devices**](#)
International Conference on Field Programmable Logic and Applications (FPL'11) (Chania, Crete, 5. September 2011 - 7. September 2011)
In: **Proceedings of the International Conference on Field-Programmable Logic and Applications**, New York, NY, USA: 2011
DOI: [10.1109/FPL.2011.56](https://doi.org/10.1109/FPL.2011.56)
BibTeX: [Download](#)
- Boppu S., Hannig F., Teich J., Pérez-Andrade R.:
[**Towards Symbolic Run-Time Reconfiguration in Tightly-Coupled Processor Arrays**](#)
2011 International Conference on Reconfigurable Computing and FPGAs (ReConFig'11) (Cancun, 30. November 2011 - 2. Dezember 2011)
In: **Proc. of ReConFig**, New York, NY, USA: 2011
DOI: [10.1109/ReConFig.2011.91](https://doi.org/10.1109/ReConFig.2011.91)

URL: <http://www.computer.org/portal/web/csd/doi/10.1109/ReConFig.2011.91>

BibTeX: [Download](#)

- [Falk J.](#), Zebelein C., Haubelt C., Teich J.:

[A rule-based static dataflow clustering algorithm for efficient embedded software synthesis](#)

14th Design, Automation and Test in Europe Conference and Exhibition, DATE 2011 (Grenoble, 14. März 2011 - 18. März 2011)

In: **Proceedings of Design, Automation and Test in Europe (DATE'11) 2011**

URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=79957549287&origin=inward>

BibTeX: [Download](#)

- Gladigau J., Gerstlauer A., Haubelt C., Streubühr M., Teich J.:

[Automatic System-Level Synthesis: From Formal Application Models to Generic Bus-Based MPSoCs](#)

In: **LNCS Transactions on High-Performance Embedded Architectures and Compilers 5** (2011), p. 1-22

ISSN: 1864-306X

BibTeX: [Download](#)

- Graf S., Streubühr M., Glaß M., Teich J.:

[Analyzing Automotive Networks using Virtual Prototypes](#)

Automotive meets Electronics (AmE), GMM Fachbericht 69 (Dortmund, Germany)

In: **Proceedings of the Automotive meets Electronics (AmE2011), GMM Fachbericht 69**, Berlin: 2011

BibTeX: [Download](#)

- Hannig F., Roloff S., Snelling G., Teich J., Zwinkau A.:

[Resource-Aware Programming and Simulation of MPSoC Architectures through Extension of X10](#)

14th International Workshop on Software and Compilers for Embedded Systems (St. Goar, 27. Juni 2011 - 28. Juni 2011)

In: **Proceedings of the 14th International Workshop on Software and Compilers for Embedded Systems**, New York, NY, USA: 2011

DOI: [10.1145/1988932.1988941](https://doi.org/10.1145/1988932.1988941)

BibTeX: [Download](#)

- Henkel J., Bauer L., Becker J., Bringmann O., Brinkschulte U., Chakraborty S., Engel M., Ernst R., Härtig H., Hedrich L., Herkersdorf A., Kapitza R., Lohmann D., Marwedel P., Platzner M., Rosenstiel W., Schlichtmann U., Spinczyk O., Tahoori M., Teich J., Wehn N., Wunderlich HJ.:

[Design and Architectures for Dependable Embedded Systems](#)

9th International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS '11) (Taipei, 9. Oktober 2011 - 14. Oktober 2011)

In: **Proceedings of the 9th International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS '11)**, New York, NY, USA:

2011

DOI: [10.1145/2039370.2039384](https://doi.org/10.1145/2039370.2039384)

BibTeX: [Download](#)

- Keinert J., Teich J.:

[Design of Image Processing Embedded Systems Using Multidimensional Data Flow](#)

Heidelberg: Springer-Verlag, 2011

(Embedded Systems)

ISBN: 978-1-4419-7181-4

URL: <http://www.springer.com/engineering/circuits+%26+systems/book/978-1-4419-7181-4>

BibTeX: [Download](#)

- Kern A., Reinhard D., Streichert T., Teich J.:

[Gateway Strategies for Embedding of Automotive CAN-frames into Ethernet-packets and Vice Versa](#)

24th International Conference on Architecture of Computing Systems (ARCS'11) (Lake Como, 24. Februar 2011 - 25. Februar 2011)

In: **Proceedings of the 24th International Conference on Architecture of Computing Systems**, Berlin; Heidelberg: 2011

DOI: [10.1007/978-3-642-19137-4_22](https://doi.org/10.1007/978-3-642-19137-4_22)

BibTeX: [Download](#)

- Kern A., Streichert T., Teich J.:

[An Automated Data Structure Migration Concept - From CAN to Ethernet/IP in Automotive Embedded Systems \(CANoverIP\)](#)

Design, Automation and Test in Europe (DATE'11) (Grenoble, 14. März 2011 - 18. März 2011)

In: **Proc. of DATE**, New York, NY, USA: 2011

URL: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=5763027

BibTeX: [Download](#)

- Kern A., Zhang H., Streichert T., Teich J.:

[Testing Switched Ethernet Networks in Automotive Embedded Systems](#)

6th IEEE International Symposium on Industrial Embedded Systems (SIES'11) (Västerås, 15. Juni 2011 - 17. Juni 2011)

In: **Proceedings of the 6th IEEE International Symposium on Industrial Embedded Systems (SIES'11)**, New York, NY, USA: 2011

DOI: [10.1109/SIES.2011.5953657](https://doi.org/10.1109/SIES.2011.5953657)

BibTeX: [Download](#)

- Kern A., Zinner H., Streichert T., Nöbauer J., Teich J.:

[Accuracy of Ethernet AVB Time Synchronization Under Varying Temperature Conditions for Automotive Networks](#)

ACM/EDAC/IEEE Design Automation Conference (DAC'11) (San Diego, California, 5. Juni 2011 - 9. Juni 2011)

In: **Proceedings of the 2011 ACM/EDAC/IEEE Design Automation Conference (DAC'11)**, New York, NY, USA: 2011

DOI: [10.1145/2024724.2024862](https://doi.org/10.1145/2024724.2024862)

BibTeX: [Download](#)

- Kiesel R., Streubühr M., Haubelt C., Löhlein O., Teich J.:

[Calibration and validation of software performance models for pedestrian detection systems](#)

2011 11th International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation, IC-SAMOS 2011 (Samos)

In: **Proceedings of the International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS XI) 2011**

DOI: [10.1109/SAMOS.2011.6045460](https://doi.org/10.1109/SAMOS.2011.6045460)

BibTeX: [Download](#)

- Kissler D., Gran D., Salcic Z., Hannig F., Teich J.:

[Scalable Many-Domain Power Gating in Coarse-grained Reconfigurable](#)

Processor Arrays

In: **IEEE Embedded Systems Letters** 3 (2011), p. 58-61

ISSN: 1943-0663

DOI: [10.1109/LES.2011.2124438](https://doi.org/10.1109/LES.2011.2124438)

BibTeX: [Download](#)

- Kissler D., Hannig F., Teich J.:

Efficient Evaluation of Power/Area/Latency Design Trade-offs for Coarse-Grained Reconfigurable Processor Arrays

In: **Journal of Low Power Electronics** 7 (2011), p. 29-40

ISSN: 1546-1998

DOI: [10.1166/jolpe.2011.1114](https://doi.org/10.1166/jolpe.2011.1114)

BibTeX: [Download](#)

- Kouveli G., Hannig F., Lupp JH., Teich J.:

Towards Resource-Aware Programming on Intel's Single-Chip Cloud Computer Processor

3rd Many-core Applications Research Community (MARC) Symposium (Ettlingen, 5. Juli 2011 - 6. Juli 2011)

In: **Proceedings of the 3rd MARC Symposium**, Karlsruhe, Germany: 2011

DOI: [10.5445/KSP/1000023937](https://doi.org/10.5445/KSP/1000023937)

BibTeX: [Download](#)

- Kutzer P., Gladigau J., Haubelt C., Teich J.:

Automatic generation of system-level virtual prototypes from streaming application models

2011 22nd IEEE International Symposium on Rapid System Prototyping: Shortening the Path from Specification to Prototype, RSP-2011 (Karlsruhe)

In: **Proceedings of the 22nd IEEE International Symposium on Rapid System Prototyping 2011**

DOI: [10.1109/RSP.2011.5929986](https://doi.org/10.1109/RSP.2011.5929986)

BibTeX: [Download](#)

- Kutzer P., Streubühr M., Haubelt C., Teich J., von Schwerin A.:

Actor-oriented Modeling of Industrial Ethernet in the Automation Domain Using SystemC

Embedded World Conference (Nueremberg, 1. März 2011 - 3. März 2011)

In: **Proceedings of the Embedded World Conference 2011**

BibTeX: [Download](#)

- Lari V., Hannig F., Teich J.:

[Distributed Resource Reservation in Massively Parallel Processor Arrays](#)

25th IEEE International Symposium on Parallel and Distributed Processing (IPDPS'11) (Anchorage, AK, 16. Mai 2011 - 20. Mai 2011)

In: **Proc. of the 25th IEEE International Symposium on Parallel and Distributed Processing**, New York, NY, USA: 2011

DOI: [10.1109/IPDPS.2011.157](https://doi.org/10.1109/IPDPS.2011.157)

BibTeX: [Download](#)

- Lari V., Narovlyanskyy A., Hannig F., Teich J.:

[Decentralized Dynamic Resource Management Support for Massively Parallel Processor Arrays](#)

22nd IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP'11) (Santa Monica, CA, 11. September 2011 - 14. September 2011)

In: **Proc. of the 22nd IEEE International Conference on Application-specific Systems, Architectures and Processors**, New York, NY, USA: 2011

DOI: [10.1109/ASAP.2011.6043240](https://doi.org/10.1109/ASAP.2011.6043240)

BibTeX: [Download](#)

- Lukasiwycz M., Glaß M., Reimann F., Teich J.:

[Opt4J - A Modular Framework for Meta-heuristic Optimization](#)

13th Annual Genetic and Evolutionary Computation Conference (GECCO'11) (Dublin, 12. Juli 2011 - 16. Juli 2011)

In: **Proc. of the 13th Annual Genetic and Evolutionary Computation Conference**, New York, NY, USA: 2011

DOI: [10.1145/2001576.2001808](https://doi.org/10.1145/2001576.2001808)

BibTeX: [Download](#)

- Marwedel P., Teich J., Kouveli G., Bacivarov I., Thiele L., Ha S., Lee C., Xu Q., Huang L.:

[Mapping of Applications to MPSoCs](#)

9th International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS'11) (Taipei, 9. Oktober 2011 - 14. Oktober 2011)

In: **Proceedings of the 9th International Conference on Hardware/Software Codesign and System Synthesis, part of ESWeek'11**, New York, NY, USA: 2011

DOI: [10.1145/2039370.2039390](https://doi.org/10.1145/2039370.2039390)

BibTeX: [Download](#)

- Membarth R., Hannig F., Teich J., Körner M., Eckert W.:

[Frameworks for GPU Accelerators: A Comprehensive Evaluation using 2D/3D Image Registration](#)

9th IEEE Symposium on Application Specific Processors (SASP) (San Diego, CA, USA, 5. Juni 2011 - 6. Juni 2011)

In: **Proceedings of the 9th IEEE Symposium on Application Specific Processors (SASP)** 2011

DOI: [10.1109/SASP.2011.5941083](https://doi.org/10.1109/SASP.2011.5941083)

BibTeX: [Download](#)

- Membarth R., Hannig F., Teich J., Körner M., Eckert W.:

[Frameworks for Multi-core Architectures: A Comprehensive Evaluation using 2D/3D Image Registration](#)

24th International Conference on Architecture of Computing Systems (ARCS) (Lake Como, 24. Februar 2011 - 25. Februar 2011)

In: **Proceedings of the 24th International Conference on Architecture of Computing Systems (ARCS)**, Heidelberg: 2011

DOI: [10.1007/978-3-642-19137-4_6](https://doi.org/10.1007/978-3-642-19137-4_6)

BibTeX: [Download](#)

- Membarth R., Hannig F., Teich J., Litz G., Hornegger H.:

[Detector Defect Correction of Medical Images on Graphics Processors](#)

SPIE: Medical Imaging : Image Processing (Lake Buena Vista, Orlando, FL, 14. Februar 2011 - 16. Februar 2011)

In: **Proceedings of the SPIE: Medical Imaging 2011: Image Processing** 2011

DOI: [10.1117/12.877656](https://doi.org/10.1117/12.877656)

BibTeX: [Download](#)

- Membarth R., Lokhmotov A., Teich J.:

[Generating GPU Code from a High-level Representation for Image Processing Kernels](#)

5th Workshop on Highly Parallel Processing on a Chip (HPPC) (Bordeaux)

In: **Proceedings of the 5th Workshop on Highly Parallel Processing on a Chip (HPPC) 2011**

BibTeX: [Download](#)

- Mühleis N., Glaß M., Zhang L., Teich J.:

[A Co-Simulation Approach for Control Performance Analysis during Design Space Exploration of Cyber-Physical Systems](#)

2nd International Conference on Cyber Physical Systems (ICCPS 2011)

In: **ACM SIGBED Review - Work-in-Progress (WiP) Session of the 2nd International Conference on Cyber Physical Systems (ICCPS 2011) 2011**

DOI: [10.1145/2000367.2000372](https://doi.org/10.1145/2000367.2000372)

BibTeX: [Download](#)

- Reimann F., Lukasiewicz M., Glaß M., Haubelt C., Teich J.:

[Symbolic system synthesis in the presence of stringent real-time constraints](#)

2011 48th ACM/EDAC/IEEE Design Automation Conference, DAC 2011 (San Diego, CA, 5. Juni 2011 - 10. Juni 2011)

URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=80052678758&origin=inward>

BibTeX: [Download](#)

- Streubühr M., Rosales R., Hasholzner R., Haubelt C., Teich J.:

[ESL Power and Performance Estimation for Heterogeneous MPSoCs Using SystemC](#)

Forum on specification and Design Languages 2011 (Oldenburg, 13. September 2011 - 15. September 2011)

In: **Forum on specification and Design Languages 2011 2011**

BibTeX: [Download](#)

- Teich J., Henkel J., Herkersdorf A., Schmitt-Landsiedel D., Schröder-Preikschat W., Snelling G.:

[Invasive Computing: An Overview](#)

In: M. Hübner and J. Becker (ed.): **Multiprocessor System-on-Chip - Hardware Design and Tool Integration**, New York: Springer, 2011, p. 241-268

ISBN: 978-1-4419-6459-5

DOI: [10.1007/978-1-4419-6460-1_11](https://doi.org/10.1007/978-1-4419-6460-1_11)

URL: <http://invasic.informatik.uni-erlangen.de/publications/invasic-overview.pdf>

BibTeX: [Download](#)

- Teich J., Ziener D.:

[Verifying the Authorship of Embedded IP Cores: Watermarking and Core Identification Techniques \(Keynote\)](#)

International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA'11) (Las Vegas)

In: **Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms 2011**

URL: <http://ersaconf.org/ersa11/program/teich.php>

BibTeX: [Download](#)

- Weichslgartner A., Wildermann S., Teich J.:

[Dynamic Decentralized Mapping of Tree-Structured Applications on NoC Architectures](#)

Fifth ACM/IEEE International Symposium on Networks-on-Chip (NOCS'11) (Pittsburgh, 1. Mai 2011 - 4. Mai 2011)

In: **Proc. Fifth ACM/IEEE International Symposium on Networks-on-Chip**, New York, NY, USA: 2011

DOI: [10.1145/1999946.1999979](https://doi.org/10.1145/1999946.1999979)

BibTeX: [Download](#)

- Wildermann S., Reimann F., Teich J., Salcic Z.:

[Operational Mode Exploration for Reconfigurable Systems with Multiple Applications](#)

International Conference on Field-Programmable Technology (FPT'11) (New Delhi, 12. Dezember 2011 - 14. Dezember 2011)

In: **Proceedings of the International Conference on Field-Programmable Technology**, New York, NY, USA: 2011

DOI: [10.1109/FPT.2011.6132693](https://doi.org/10.1109/FPT.2011.6132693)

BibTeX: [Download](#)

- Wildermann S., Reimann F., Ziener D., Teich J.:

[Symbolic Design Space Exploration for Multi-Mode Reconfigurable Systems](#)

9th International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS'11) (Taipei, 9. Oktober 2011 - 14. Oktober 2011)

In: **Proceedings of the 9th International Conference on Hardware/Software Codesign and System Synthesis, part of ESWeek'11**, New York, NY, USA: 2011

DOI: [10.1145/2039370.2039393](https://doi.org/10.1145/2039370.2039393)

BibTeX: [Download](#)

- Wildermann S., Ziener D., Teich J.:

[Unifying Partitioning and Placement for SAT-based Exploration of Heterogeneous Reconfigurable SoCs](#)

International Conference on Field Programmable Logic and Applications (FPL'11) (Chania, Crete, 5. September 2011 - 7. September 2011)

In: **Proc. of the International Conference on Field Programmable Logic and Applications**, New York, NY, USA: 2011

DOI: [10.1109/FPL.2011.85](https://doi.org/10.1109/FPL.2011.85)

BibTeX: [Download](#)

- Ziener D., Wildermann S., Oetken A., Weichslgartner A., Teich J.:

[A Flexible Smart Camera System based on a Partially Reconfigurable Dynamic FPGA-SoC](#)

Workshop on Computer Vision on Low-Power Reconfigurable Architectures at FPL 2011 (Chania, Crete, 4. September 2011 - 4. September 2011)

In: **Proceedings of the Workshop on Computer Vision on Low-Power Reconfigurable Architectures at FPL 2011** 2011

BibTeX: [Download](#)

- Ziermann T., Salcic Z., Teich J.:

[DynOAA - Dynamic Offset Adaptation Algorithm for Improving Response Times of CAN Systems](#)

Design, Automation and Test in Europe (DATE'11) (Grenoble, 14. März 2011 - 18. März 2011)

In: **Proc. of DATE**, New York, NY, USA: 2011

URL: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=5763272

BibTeX: [Download](#)

- Ziermann T., Salcic Z., Teich J.:
[Self-organized Message Scheduling for Asynchronous Distributed Embedded Systems](#)
8th International Conference on Autonomic and Trusted Computing (ATC'11)
(Banff, 2. September 2011 - 4. September 2011)
In: **Proc. of the 8th International Conference on Autonomic and Trusted Computing**, Heidelberg: 2011
DOI: [10.1007/978-3-642-23496-5_10](https://doi.org/10.1007/978-3-642-23496-5_10)
BibTeX: [Download](#)
 - Ziermann T., Schmidt B., Mühlenthaler M., Ziener D., Angermeier J., Teich J.:
[An FPGA Implementation of a Threat-based Strategy for Connect6](#)
International Conference on Field-Programmable Technology (FPT'11) (New Delhi, 12. Dezember 2011 - 14. Dezember 2011)
In: **Proceedings of the International Conference on Field-Programmable Technology**, New York, NY, USA: 2011
DOI: [10.1109/FPT.2011.6133250](https://doi.org/10.1109/FPT.2011.6133250)
BibTeX: [Download](#)
 - Ziermann T., Wildermann S., Teich J.:
[OrganicBus: Organic Self-organising Bus-Based Communication Systems](#)
In: **Organic Computing - A Paradigm Shift for Complex Systems**, Basel: Birkhäuser Verlag, 2011, p. 489-501
ISBN: 978-3-0348-0130-0
DOI: [10.1007/978-3-0348-0130-0_32](https://doi.org/10.1007/978-3-0348-0130-0_32)
BibTeX: [Download](#)
- 2010**
- Ahmadinia A., Angermeier J., Fekete SP., Kamphans T., Koch D., Majer M., Schweer N., Teich J., Tessars C., Van Der Veen JC.:
[ReCoNodes-optimization methods for module scheduling and placement on reconfigurable hardware devices](#)
Springer Netherlands, 2010
ISBN: 9789048134847

DOI: [10.1007/978-90-481-3485-4_10](https://doi.org/10.1007/978-90-481-3485-4_10)

BibTeX: [Download](#)

- Angermeier J., Bobda C., Majer M., Teich J.:
[Erlangen slot machine: An FPGA-based dynamically reconfigurable computing platform](#)
Springer Netherlands, 2010
ISBN: 9789048134847
DOI: [10.1007/978-90-481-3485-4_3](https://doi.org/10.1007/978-90-481-3485-4_3)
BibTeX: [Download](#)
- Angermeier J., Teich J., Kamphans T., Fekete SP.:
[Virtual Area Management: Multitasking on Dynamically Partially Reconfigurable Devices](#)
17th Reconfigurable Architectures Workshop (RAW'10) (Atlanta, 19. April 2010 - 23. April 2010)
In: **Proc. 17th Reconfigurable Architectures Workshop 2010**
DOI: [10.1109/IPDPSW.2010.5470754](https://doi.org/10.1109/IPDPSW.2010.5470754)
BibTeX: [Download](#)
- Angermeier J., Wildermann S., Sibirko E., Teich J.:
[Placing Streaming Applications with Similarities on Dynamically Partially Reconfigurable Architectures](#)
International Conference on ReConFigurable Computing and FPGAs (ReConFig'10) (Cancun, 13. Dezember 2010 - 15. Dezember 2010)
In: **Proc. International Conference on ReConFigurable Computing and FPGAs 2010**
DOI: [10.1109/ReConFig.2010.52](https://doi.org/10.1109/ReConFig.2010.52)
BibTeX: [Download](#)
- Chakraborty S., Ramesh S., Teich J.:
[Model-based analysis, synthesis and testing of automotive hardware/software architectures](#)
6th Embedded Systems Week 2010, ESWEEK 2010 - 10th ACM International Conference on Compilers, Architecture and Synthesis for Embedded Systems, EMSOFT'10 (Scottsdale, AZ)

DOI: [10.1145/1879021.1879061](https://doi.org/10.1145/1879021.1879061)

BibTeX: [Download](#)

- Charot F., Hannig F., Teich J., Wolinski C.:
[**Proc. 21st IEEE International Conference on Application-specific Systems, Architectures, and Processors**](#)
New York, NY, USA: IEEE Press, 2010
ISBN: 978-1-4244-6967-3
DOI: [10.1109/ASAP.2010.5540766](https://doi.org/10.1109/ASAP.2010.5540766)
BibTeX: [Download](#)
- [Falk J.](#), Keinert J., Haubelt C., Teich J., Zebelein C.:
[**Integrated Modeling Using Finite State Machines and Dataflow Graphs**](#)
In: Bhattacharyya S., Deprettere E., Leupers R., Takala J. (ed.): **Handbook of Signal Processing Systems**, Boston, MA: Springer, 2010, p. 1041-1075
ISBN: 978-1-4419-6344-4
DOI: [10.1007/978-1-4419-6345-1_36](https://doi.org/10.1007/978-1-4419-6345-1_36)
BibTeX: [Download](#)
- [Falk J.](#), Zebelein C., Haubelt C., Teich J., Dorsch R.:
[**Integrating Hardware/Firmware Verification Efforts Using SystemC High-Level Models**](#)
3. ITG/GI/GMM Workshop für Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (Dresden, 22. Februar 2010 - 24. Februar 2010)
In: **3. ITG/GI/GMM Workshop für Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen 2010**
BibTeX: [Download](#)
- [Falk J.](#), Zebelein C., Keinert J., Haubelt C., Teich J., Bhattacharyya SS.:
[**Analysis of systemc actor networks for efficient synthesis**](#)
In: **ACM Transactions on Embedded Computing Systems** 10 (2010), Article No.: 18
ISSN: 1539-9087
DOI: [10.1145/1880050.1880054](https://doi.org/10.1145/1880050.1880054)
BibTeX: [Download](#)

- Gladigau J., Gerstlauer A., Haubelt C., Streubühr M., Teich J.:
[**A system-level synthesis approach from formal application models to generic bus-based MPSoCs**](#)
2010 10th International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation, IC-SAMOS 2010 (Samos, 19. Juli 2010 - 22. Juli 2010)
In: **Proceedings of the International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS) 2010**
DOI: [10.1109/ICCSAMOS.2010.5642076](https://doi.org/10.1109/ICCSAMOS.2010.5642076)
BibTeX: [Download](#)
- Glaß M., Lukasiwycz M., Haubelt C., Teich J.:
[**Lifetime Reliability Optimization for Embedded Systems: A System-Level Approach**](#)
IEEE International Workshop on Reliability Aware System Design and Test (RASDAT '10) (Bangalore, 7. Januar 2010 - 8. Januar 2010)
In: **Proceedings of IEEE International Workshop on Reliability Aware System Design and Test (RASDAT '10) 2010**
BibTeX: [Download](#)
- Glaß M., Lukasiwycz M., Haubelt C., Teich J.:
[**Towards scalable system-level reliability analysis**](#)
47th Design Automation Conference, DAC '10 (Anaheim, CA, 13. Juni 2010 - 18. Juni 2010)
DOI: [10.1145/1837274.1837334](https://doi.org/10.1145/1837274.1837334)
BibTeX: [Download](#)
- Glaß M., Lukasiwycz M., Reimann F., Haubelt C., Teich J.:
[**Symbolic system level reliability analysis**](#)
2010 IEEE/ACM International Conference on Computer-Aided Design, ICCAD 2010 (San Jose, CA, 7. November 2010 - 11. November 2010)
In: **Proceedings of the International Conference on Computer-Aided Design (ICCAD) 2010**
DOI: [10.1109/ICCAD.2010.5654134](https://doi.org/10.1109/ICCAD.2010.5654134)
BibTeX: [Download](#)

- Hannig F., Schmid M., Teich J., Hornegger H.:
[**A Deeply Pipelined and Parallel Architecture for Denoising Medical Images**](#)
IEEE International Conference on Field Programmable Technology (FPT'10) (Beijing, 8. Dezember 2010 - 10. Dezember 2010)
In: **Proc. IEEE International Conference on Field Programmable Technology 2010**
DOI: [10.1109/FPT.2010.5681464](https://doi.org/10.1109/FPT.2010.5681464)
BibTeX: [Download](#)
- Haubelt C., Koch D., Reimann F., Streichert T., Teich J.:
[**ReCoNets-design methodology for embedded systems consisting of small networks of reconfigurable nodes and connections**](#)
Springer Netherlands, 2010
ISBN: 9789048134847
DOI: [10.1007/978-90-481-3485-4_11](https://doi.org/10.1007/978-90-481-3485-4_11)
BibTeX: [Download](#)
- Haubelt C., Teich J.:
[**Digitale Hardware/Software-Systeme: Spezifikation und Verifikation**](#)
Berlin, Heidelberg: Springer-Verlag, 2010
BibTeX: [Download](#)
- Kern A., Schmutzler C., Streichert T., Hübner M., Teich J.:
[**Network bandwidth optimization of ethernet-based streaming applications in automotive embedded systems**](#)
2010 19th International Conference on Computer Communications and Networks, ICCCN 2010 (Zurich, 2. August 2010 - 5. August 2010)
In: **Proceedings of the International Conference on Computer Communication Networks (ICCCN) 2010 – Track on Network Algorithms, Performance Evaluation and Theory (NAPET) 2010**
DOI: [10.1109/ICCCN.2010.5560142](https://doi.org/10.1109/ICCCN.2010.5560142)
BibTeX: [Download](#)
- Kiesel R., Löhlein O., Terzis A., Streubühr M., Haubelt C., Teich J.:
[**Actor-oriented Modeling of Driver Assistance Systems for Efficient Multi-Core ECU Implementation**](#)
Methoden und Beschreibungssprachen zur Modellierung und Verifikation von

Schaltungen und Systemen (Dresden)

In: **Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen 2010**

BibTeX: [Download](#)

- Lukasiewicz M., Glaß M., Teich J.:

[Robust Design of Embedded Systems](#)

Design, Automation and Test in Europe (DATE'10) (Dresden, 8. März 2010 - 12. März 2010)

In: **Proc. Design, Automation and Test in Europe 2010**

BibTeX: [Download](#)

- May M., Wehn N., Bouajila A., Zeppenfeld J., Stechele W., Herkersdorf A., Ziener D., Teich J.:

[A Rapid Prototyping System for Error-Resilient Multi-Processor Systems-on-Chip](#)

Design, Automation and Test in Europe (DATE'10) (Dresden, 8. März 2010 - 12. März 2010)

In: **Proc. Design, Automation and Test in Europe 2010**

BibTeX: [Download](#)

- Membarth R., Hannig F., Teich J., Körner M., Eckert W.:

[Comparison of Parallelization Frameworks for Shared Memory Multi-Core Architectures](#)

Embedded World Conference (Nuremberg, 3. März 2010 - 5. März 2010)

In: **Proc. Embedded World Conference 2010**

BibTeX: [Download](#)

- Oetken A., Wildermann S., Teich J., Koch D.:

[A bus-based SoC architecture for flexible module placement on reconfigurable FPGAs](#)

20th International Conference on Field Programmable Logic and Applications, FPL 2010 (Milano)

In: **Proceedings of International Conference on Field-Programmable Logic and Applications (FPL'10) 2010**

DOI: [10.1109/FPL.2010.54](https://doi.org/10.1109/FPL.2010.54)

BibTeX: [Download](#)

- Platzner M., Teich J., Wehn N.:
[Dynamically Reconfigurable Systems - Architectures, Design Methods and Applications](#)
Heidelberg: Springer, 2010
ISBN: 978-90-481-3484-7
DOI: [10.1007/978-90-481-3485-4](https://doi.org/10.1007/978-90-481-3485-4)
BibTeX: [Download](#)
- Reimann F., Kern A., Haubelt C., Streichert T., Teich J.:
[Echtzeitanalyse Ethernet-basierter E/E-Architekturen im Automobil](#)
Automotive meets Electronics (AmE'10) (Dortmund, Germany)
In: **GMM-Fachbericht - Automotive meets Electronics**, Berlin: 2010
BibTeX: [Download](#)
(Techreport)
- Schmid M., Hannig F., Teich J., Diefenbach R., Pettendorf R., Hornegger H.:
[Discourse on Extending Embedded Medical Image Processing Systems Using the High Speed Serial RapidIO Interconnect](#)
Embedded World Conference (Nuremberg, 3. März 2010 - 5. März 2010)
In: **Proceedings of the Embedded World Conference 2010**
BibTeX: [Download](#)
- Sim JE., Wong WF., Walla G., Ziermann T., Teich J.:
[Interprocedural Placement-Aware Configuration Prefetching for FPGA-based Systems](#)
18th Annual International IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'10) (Charlotte, North Carolina, 2. Mai 2010 - 4. Mai 2010)
In: **Proc. 18th Annual International IEEE Symposium on Field-Programmable Custom Computing Machines 2010**
DOI: [10.1109/FCCM.2010.35](https://doi.org/10.1109/FCCM.2010.35)
BibTeX: [Download](#)
- Streubühr M., Gladigau J., Haubelt C., Teich J.:
[Efficient approximately-timed performance modeling for architectural exploration of MPSoCs](#)
2010

ISBN: 9789048193035

DOI: [10.1007/978-90-481-9304-2_4](https://doi.org/10.1007/978-90-481-9304-2_4)

BibTeX: [Download](#)

- Teich J., Haubelt C., Eberl M., Reimann F., Glaß M.:
[Improving platform-based system synthesis by satisfiability Modulo theories solving](#)
6th Embedded Systems Week, ESWEEK 2010 - 8th IEEE/ACM International Conference on Hardware/Software-Co-Design and System Synthesis, CODES+ISSS'10 (Scottsdale, AZ, 24. Oktober 2010 - 29. Oktober 2010)
In: **Proceedings of the 8th International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) 2010**
DOI: [10.1145/1878961.1878986](https://doi.org/10.1145/1878961.1878986)
BibTeX: [Download](#)
- Wildermann S., Oetken A., Teich J., Salcic Z.:
[Self-organizing computer vision for robust object tracking in smart cameras](#)
7th International Conference on Autonomic and Trusted Computing, ATC 2010 (Xi'an, 26. Oktober 2010 - 29. Oktober 2010)
In: **Proceedings of the 7th International Conference on Autonomic and Trusted Computing 2010**
DOI: [10.1007/978-3-642-16576-4_1](https://doi.org/10.1007/978-3-642-16576-4_1)
BibTeX: [Download](#)
- Zebelein C., [Falk J.](#), Haubelt C., Teich J., Dorsch R.:
[Efficient high-level modeling in the networking domain](#)
Design, Automation and Test in Europe Conference and Exhibition, DATE 2010 (Dresden, 8. März 2010 - 12. März 2010)
In: **Proceedings of Design, Automation and Test in Europe (DATE 2010) 2010**
URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=77953092909&origin=inward>
BibTeX: [Download](#)
- Ziener D., Baueregger F., Teich J.:
[Multiplexing Methods for Power Watermarking](#)
IEEE Int. Symposium on Hardware-Oriented Security and Trust (HOST'10)

(Anaheim, 13. Juni 2010 - 14. Juni 2010)

In: **Proc. IEEE Int. Symposium on Hardware-Oriented Security and Trust 2010**

DOI: [10.1109/HST.2010.5513118](https://doi.org/10.1109/HST.2010.5513118)

BibTeX: [Download](#)

- Ziener D., Baueregger F., Teich J.:

[Using the Power Side Channel of FPGAs for Communication](#)

18th Annual International IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'10) (Charlotte, North Carolina, 2. Mai 2010 - 4. Mai 2010)

In: **Proc. 18th Annual International IEEE Symposium on Field-Programmable Custom Computing Machines 2010**

DOI: [10.1109/FCCM.2010.43](https://doi.org/10.1109/FCCM.2010.43)

BibTeX: [Download](#)

- Ziener D., Schmid M., Teich J.:

[Robustness Analysis of Watermark Verification Techniques for FPGA Netlist Cores](#)

In: **Design Methodologies for Secure Embedded Systems**, Berlin: Springer Verlag, 2010, p. 105-127 (Lecture Notes in Electrical Engineering, Vol.78)
ISBN: 978-3-642-16766-9

DOI: [10.1007/978-3-642-16767-6_6](https://doi.org/10.1007/978-3-642-16767-6_6)

BibTeX: [Download](#)

- Ziener D., Teich J.:

[New Directions for FPGA IP Core Watermarking and Identification](#)

Dagstuhl Seminar 10281

In: **Dagstuhl Seminar 10281 Proceedings 2010**

BibTeX: [Download](#)

- Ziermann T., Mühleis N., Wildermann S., Teich J.:

[A self-organizing distributed reinforcement learning algorithm to achieve fair bandwidth allocation for priority-based bus communication](#)

2010 13th IEEE International Symposium on Object/Component/Service-Oriented Real-Time Distributed Computing Workshops, ISORC Workshops 2010 (Carmona, Sevilla, 11. Mai 2010 - 11. Mai 2010)

In: **Proceedings of the 1st IEEE Workshop on Self-Organizing Real-Time systems (SORT 2010)** 2010

DOI: [10.1109/ISORCW.2010.18](https://doi.org/10.1109/ISORCW.2010.18)

BibTeX: [Download](#)

- Ziermann T., Teich J.:

[Adaptive Traffic Scheduling Techniques for Mixed Real-Time and Streaming Applications on Reconfigurable Hardware](#)

17th Reconfigurable Architectures Workshop (RAW'10) (Atlanta, 19. April 2010 - 23. April 2010)

In: **Proc. 17th Reconfigurable Architectures Workshop** 2010

DOI: [10.1109/IPDPSW.2010.5470738](https://doi.org/10.1109/IPDPSW.2010.5470738)

BibTeX: [Download](#)

- Ziermann T., Teich J.:

[Electromagnetic Compatibility \(EMC\) of CAN+](#)

Automotive meets Electronics (AmE'10) (Dortmund, 15. April 2010 - 16. April 2010)

In: **GMM-Fachbericht - Automotive meets Electronics**, Berlin: 2010

BibTeX: [Download](#)

2009

- Arifin F., Amouri A., Hannig F., Teich J.:

[FPGA Implementation of an Invasive Computing Architecture](#)

IEEE International Conference on Field Programmable Technology (FPT) (Sydney, 9. Dezember 2009 - 11. Dezember 2009)

In: **Proceedings of the IEEE International Conference on Field Programmable Technology** 2009

DOI: [10.1109/FPT.2009.5377633](https://doi.org/10.1109/FPT.2009.5377633)

BibTeX: [Download](#)

- Arifin F., Membarth R., Amouri A., Hannig F., Teich J.:

[FSM-Controlled Architectures for Linear Invasion](#)

17th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) (Florianópolis)

In: **Proceedings of the 17th IFIP/IEEE International Conference on Very**

Large Scale Integration 2009

BibTeX: [Download](#)

- Dutt N., Teich J.:
[CODES+ISSS 2007 guest editors' introduction](#)
In: **Design Automation For Embedded Systems** 13 (2009), p. 51-52
ISSN: 0929-5585
DOI: [10.1007/s10617-008-9036-9](https://doi.org/10.1007/s10617-008-9036-9)
BibTeX: [Download](#)
- Dutta H., Hannig F., Teich J.:
[Performance Matching of Hardware Acceleration Engines for Heterogeneous MPSoC using Modular Performance Analysis](#)
22nd International Conference on Architecture of Computing Systems (ARCS) (Delft, 10. März 2009 - 13. März 2009)
In: **Proceedings of the 22nd International Conference on Architecture of Computing Systems** 2009
DOI: [10.1007/978-3-642-00454-4_23](https://doi.org/10.1007/978-3-642-00454-4_23)
BibTeX: [Download](#)
- Dutta H., Kissler D., Hannig F., Kupriyanov O., Teich J., Pottier B.:
[A Holistic Approach for Tightly Coupled Reconfigurable Parallel Processors](#)
In: **Microprocessors and Microsystems** 33 (2009), p. 53-62
ISSN: 0141-9331
DOI: [10.1016/j.micpro.2008.08.007](https://doi.org/10.1016/j.micpro.2008.08.007)
BibTeX: [Download](#)
- Dutta H., Zhai J., Hannig F., Teich J.:
[Impact of loop tiling on the controller logic of acceleration engines](#)
2009 20th IEEE International Conference on Application-specific Systems, Architectures and Processors, ASAP 2009 (Boston, MA, 7. Juli 2009 - 9. Juli 2009)
In: **Proceedings of 20th IEEE International Conference on Application-specific Systems, Architectures, and Processors (ASAP)** 2009
DOI: [10.1109/ASAP.2009.21](https://doi.org/10.1109/ASAP.2009.21)
BibTeX: [Download](#)

- Dutta H., Zhai J., Hannig F., Teich J.:
[Impact of Loop Tiling on the Controller Logic of Hardware Acceleration Engines](#)
20th IEEE International Conference on Application-specific Systems, Architectures, and Processors (ASAP) (Boston, MA, 7. Juli 2009 - 9. Juli 2009)
In: **Proceedings of the 20th IEEE International Conference on Application-specific Systems, Architectures, and Processors 2009**
BibTeX: [Download](#)
- Gerstlauer A., Haubelt C., Pimentel A., Stefanov T., Gajski D., Teich J.:
[Electronic System-Level Synthesis Methodologies](#)
In: **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 28** (2009), p. 1517-1530
ISSN: 0278-0070
DOI: [10.1109/TCAD.2009.2026356](#)
BibTeX: [Download](#)
- Gladigau J., Haubelt C., Streubühr M., Teich J., Schneider A., Knäblein J., Lindig M.:
[Testfallgenerierung für SystemC-Designs mit abstrakten Modellbeschreibungen](#)
Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (Berlin, 2. März 2009 - 4. März 2009)
In: **Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen 2009**
BibTeX: [Download](#)
- Gladigau J., Haubelt C., Teich J.:
[Symbolic scheduling of SystemC dataflow designs](#)
In: M. Radetzki (ed.): **Languages for Embedded Systems and their Applications**, Springer, 2009, p. 183-199 (Lecture Notes in Electrical Engineering, Vol.36)
ISBN: 9781402097133
DOI: [10.1007/978-1-4020-9714-0_12](#)
BibTeX: [Download](#)

- Glaß M., Haubelt C., Lukasiewicz M., Teich J.:
[Incorporating graceful degradation into embedded system design](#)
2009 Design, Automation and Test in Europe Conference and Exhibition, DATE '09 (Nice, 20. April 2009 - 24. April 2009)
In: **Proceedings of Design, Automation and Test in Europe (DATE 2009)**
2009
URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=70350062092&origin=inward>
BibTeX: [Download](#)
- Glaß M., Lukasiewicz M., Teich J., Bordoloi U., Chakraborty S.:
[Designing Heterogeneous ECU Networks via Compact Architecture Encoding and Hybrid Timing Analysis](#)
ACM/EDAC/IEEE Design Automation Conference (DAC'09) (San Francisco, 26. Juli 2009 - 31. Juli 2009)
In: **Proc. 2009 ACM/EDAC/IEEE Design Automation Conference 2009**
BibTeX: [Download](#)
- Hannig F., Dutta H., Teich J.:
[Parallelization Approaches for Hardware Accelerators - Loop Unrolling versus Loop Partitioning](#)
22nd International Conference on Architecture of Computing Systems (ARCS) (Delft, 10. März 2009 - 13. März 2009)
In: **Proceedings of the 22nd International Conference on Architecture of Computing Systems 2009**
DOI: [10.1007/978-3-642-00454-4_5](https://doi.org/10.1007/978-3-642-00454-4_5)
BibTeX: [Download](#)
- Keinert J., Dutta H., Hannig F., Haubelt C., Teich J.:
[Model-based synthesis and optimization of static multi-rate image processing algorithms](#)
2009 Design, Automation and Test in Europe Conference and Exhibition, DATE '09 (Nice, 20. April 2009 - 24. April 2009)
In: **Proceedings of Design, Automation and Test in Europe (DATE 2009)**
2009

URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=70350072695&origin=inward>

BibTeX: [Download](#)

- Keinert J., Haubelt C., Teich J.:

[Data Flow Based System Level Design and Analysis of Concurrent Image Processing Applications](#)

DATE'09 Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications (Nice)

In: **Proceedings of DATE'09 Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications 2009**

BibTeX: [Download](#)

- Keinert J., Streubühr M., Schlichter T., [Falk J.](#), Gladigau J., Teich J., Haubelt C., Meredith M.:

[SYSTEMCODESIGNER - An Automatic ESL Synthesis Approach by Design Space Exploration and Behavioral Synthesis for Streaming Applications](#)

In: **ACM Transactions on Design Automation of Electronic Systems 14** (2009), p. 1-23

ISSN: 1084-4309

DOI: [10.1145/1455229.1455230](https://doi.org/10.1145/1455229.1455230)

BibTeX: [Download](#)

- Kissler D., Strawetz A., Hannig F., Teich J.:

[Power-efficient Reconfiguration Control in Coarse-grained Dynamically Reconfigurable Architectures](#)

In: **Journal of Low Power Electronics 5** (2009), p. 96-105

ISSN: 1546-1998

DOI: [10.1166/jolpe.2009.1008](https://doi.org/10.1166/jolpe.2009.1008)

BibTeX: [Download](#)

- Koch D., Beckhoff C., Teich J.:

[A Communication Architecture for Complex Runtime Reconfigurable Systems and its Implementation on Spartan-3 FPGAs](#)

17th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA'09) (Monterey, California)

In: **Proc. 17th ACM/SIGDA International Symposium on Field-Programmable**

Gate Arrays 2009

BibTeX: [Download](#)

- Koch D., Beckhoff C., Teich J.:

[Minimizing Internal Fragmentation by Fine-grained Two-dimensional Module Placement for Runtime Reconfigurable Systems](#)

17th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'09) (Napa, CA, 5. April 2009 - 7. April 2009)

In: **Proc. 17th Annual IEEE Symposium on Field-Programmable Custom Computing Machines 2009**

DOI: [10.1109/FCCM.2009.40](https://doi.org/10.1109/FCCM.2009.40)

BibTeX: [Download](#)

- Lari V., Hannig F., Teich J.:

[System Integration of Tightly-Coupled Reconfigurable Processor Arrays and Evaluation of Buffer Size Effects on Their Performance](#)

4th International Symposium on Embedded Multicore Systems-on-Chip (MCSoc) (Vienna, 22. September 2009 - 25. September 2009)

In: **Proceedings of the 4th International Symposium on Embedded Multicore Systems-on-Chip 2009**

DOI: [10.1109/ICPPW.2009.72](https://doi.org/10.1109/ICPPW.2009.72)

BibTeX: [Download](#)

- Lukasiewicz M., Glaß M., Milbredt P., Teich J.:

[FlexRay Schedule Optimization of the Static Segment](#)

7th International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) (Grenoble, 11. Oktober 2009 - 16. Oktober 2009)

In: **Proc. 7th International Conference on Hardware/Software Codesign and System Synthesis 2009**

DOI: [10.1145/1629435.1629485](https://doi.org/10.1145/1629435.1629485)

BibTeX: [Download](#)

- Lukasiewicz M., Glaß M., Teich J.:

[Exploiting Data-Redundancy in Reliability-Aware Networked Embedded System Design](#)

7th International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) (Grenoble, 11. Oktober 2009 - 16. Oktober 2009)

In: **Proc. 7th International Conference on Hardware/Software Codesign and System Synthesis 2009**

DOI: [10.1145/1629435.1629468](https://doi.org/10.1145/1629435.1629468)

BibTeX: [Download](#)

- Lukasiwycz M., Streubühr M., Glaß M., Haubelt C., Teich J.:
[**Combined system synthesis and communication architecture exploration for MPSoCs**](#)
2009 Design, Automation and Test in Europe Conference and Exhibition, DATE '09 (Nice, 20. April 2009 - 24. April 2009)
In: **Proceedings of Design, Automation and Test in Europe (DATE 2009) 2009**
URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=70350043908&origin=inward>
BibTeX: [Download](#)
- Membarth R., Hannig F., Dutta H., Teich J.:
[**Efficient Mapping of Multiresolution Image Filtering Algorithms on Graphics Processors**](#)
9th International Workshop on Systems, Architectures, Modeling, and Simulation (SAMOS Workshop) (Island of Samos, 20. Juli 2009 - 23. Juli 2009)
In: **Proceedings of the 9th International Workshop on Systems, Architectures, Modeling, and Simulation (SAMOS), Berlin / Heidelberg: 2009**
DOI: [10.1007/978-3-642-03138-0_31](https://doi.org/10.1007/978-3-642-03138-0_31)
BibTeX: [Download](#)
- Membarth R., Hannig F., Dutta H., Teich J.:
[**Optimization Flow for Algorithm Mapping on Graphics Cards**](#)
Advanced Computer Architecture and Compilation for Embedded Systems (ACACES) (Barcelona, 12. Juli 2009 - 18. Juli 2009)
In: **Proceedings of ACACES 2009 Poster Abstracts: Advanced Computer Architecture and Compilation for Embedded Systems 2009**
BibTeX: [Download](#)
- Membarth R., Kutzer P., Dutta H., Hannig F., Teich J.:
[**Acceleration of multiresolution imaging algorithms: A comparative study**](#)

2009 20th IEEE International Conference on Application-specific Systems, Architectures and Processors, ASAP 2009 (Boston, MA, 7. Juli 2009 - 9. Juli 2009)

In: **Proceedings of the 20th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP) 2009**

DOI: [10.1109/ASAP.2009.8](https://doi.org/10.1109/ASAP.2009.8)

BibTeX: [Download](#)

- Schöber V., Bringmann O., Herkersdorf A., Stechele W., Wehn N., May M., Zie-ner D., Bouajila A., Baldin D., Zeppenfeld J., Sanders B., Teich J., Sebastian M., Ernst R., Treytnar D.:

[AIS-Autonomous Integrated Systems](#)

In: **newsletter edacentrum 4** (2009), p. 5-13

ISSN: 1862-2283

BibTeX: [Download](#)

- Sim JE., Wong WF., Teich J.:

[Optimal Placement-aware Trace-based Scheduling of Hardware Reconfigu-rations for FPGA Accelerators](#)

17th IEEE Symposium on Field Programmable Custom Computing Machines (FCCM'09) (Napa, CA, 5. April 2009 - 7. April 2009)

In: **Proc. 17th IEEE Symposium on Field Programmable Custom Computing Machines 2009**

DOI: [10.1109/FCCM.2009.49](https://doi.org/10.1109/FCCM.2009.49)

BibTeX: [Download](#)

- Streubühr M., Gladigau J., Haubelt C., Teich J.:

[Efficient approximately-timed performance modeling for architectural explo-ration of MPSoCs](#)

2009 Forum on Specification and Design Languages, FDL 2009 (Sophia Antipo-lis, 22. September 2009 - 24. September 2009)

In: **Forum on specification and Design Languages 2009 2009**

URL: <https://www.scopus.com/inward/record.url?partne-riD=HzOxMe3b&scp=77951563792&origin=inward>

BibTeX: [Download](#)

- Streubühr M., Haubelt C., Teich J.:

[System Level Performance Simulation for Heterogeneous Multi-Processor](#)

Architectures

1st HiPEAC Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools (RAPIDO), in conjunction with the 4th HiPEAC Conference (Paphos, 25. Januar 2009 - 25. Januar 2009)

In: **1st HiPEAC Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools (RAPIDO), in conjunction with the 4th HiPEAC Conference 2009**

BibTeX: [Download](#)

- Streubühr M., Jäntsch M., Haubelt C., Teich J.:

[From Model-based Design to Virtual Prototypes for Automotive Applications](#)

Embedded World Conference (Nuremberg, 3. März 2009 - 5. März 2009)

In: **Proceedings of the Embedded World Conference 2009**

BibTeX: [Download](#)

- Teich J., Angermeier J., Amouri A.:

[General methodology for mapping iterative approximation algorithms to adaptive dynamically partially reconfigurable systems](#)

FPL 09: 19th International Conference on Field Programmable Logic and Applications (Prague, 31. August 2009 - 31. August 2009)

In: **Proc. 19th International Conference on Field-Programmable Logic and Applications 2009**

DOI: [10.1109/FPL.2009.5272281](https://doi.org/10.1109/FPL.2009.5272281)

BibTeX: [Download](#)

- Teich J., Beckhoff C., Koch D.:

[A communication architecture for complex runtime systems and its implementation on spartan-3 FPGAs](#)

7th ACM SIGDA International Symposium on Field-Programmable Gate Arrays, FPGA'09 (Monterey, CA)

In: **Proceedings of the 17th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2009) 2009**

DOI: [10.1145/1508128.1508170](https://doi.org/10.1145/1508128.1508170)

BibTeX: [Download](#)

- Teich J., Beckhoff C., Koch D.:
[Hardware decompression techniques for FPGA-based embedded systems](#)
In: **ACM Transactions on Reconfigurable Technology and Systems 2** (2009),
Article No.: 9
ISSN: 1936-7406
DOI: [10.1145/1534916.1534919](https://doi.org/10.1145/1534916.1534919)
BibTeX: [Download](#)
- Wildermann S., Walla G., Ziermann T., Teich J.:
[Self-Organizing Multi-cue Fusion for FPGA-based Embedded Imaging](#)
19th International Conference on Field-Programmable Logic and Applications (FPL'09) (Prague, 31. August 2009 - 2. September 2009)
In: **Proc. 19th International Conference on Field-Programmable Logic and Applications 2009**
DOI: [10.1109/FPL.2009.5272523](https://doi.org/10.1109/FPL.2009.5272523)
BibTeX: [Download](#)
- Wildermann S., Ziermann T., Teich J.:
[Run time Mapping of Adaptive Applications onto Homogeneous NoC-based Reconfigurable Architectures](#)
The International Conference on Field-Programmable Technology (FPT'09) (Sydney)
In: **Proc. 2009 International Conference on Field-Programmable Technology 2009**
BibTeX: [Download](#)
- Wildermann S., Ziermann T., Teich J.:
[Self-Organizing Bandwidth Sharing in Priority-based Medium Access](#)
Third IEEE International Conference on Self-Adaptive and Self-Organizing Systems (SASO'09) (San Francisco, 14. September 2009 - 18. September 2009)
In: **Proc. 3rd IEEE International Conference on Self-Adaptive and Self-Organizing Systems 2009**
DOI: [10.1109/SASO.2009.18](https://doi.org/10.1109/SASO.2009.18)
BibTeX: [Download](#)

- Ziener D., Teich J.:
[Concepts for run-time and error-resilient control flow checking of embedded RISC CPUs](#)
In: **International Journal of Autonomous and Adaptive Communications Systems** 2 (2009), p. 256-275
ISSN: 1754-8632
DOI: [10.1504/IJAACS.2009.026785](https://doi.org/10.1504/IJAACS.2009.026785)
BibTeX: [Download](#)
- Ziermann T., Teich J., Wildermann S.:
[CAN+: Techniques and Prototype for Achieving Increased Data Rates on the Basis of Common CAN Bus Structures](#)
The 9th Stuttgart, International Symposium (Stuttgart)
In: **Proc. 9th Stuttgart, International Symposium 2009**
BibTeX: [Download](#)
- Ziermann T., Wildermann S., Teich J.:
[CAN+: A New Backward-compatible Controller Area Network \(CAN\) Protocol with up to 16x Higher Data Rates](#)
Design, Automation and Test in Europe (DATE'09) (Nice, 20. April 2009 - 24. April 2009)
In: **Proc. Design, Automation and Test in Europe 2009**
BibTeX: [Download](#)

2008

- Ahmadinia Ali, Fekete Sándor, Göhringer Diana, Majer Mateusz, Teich Jürgen, van der Veen Jan:
[Offline and Online Aspects of Defragmenting the Module Layout of a Partially Reconfigurable Device](#)
In: **IEEE Transactions on Very Large Scale Integration (Vlsi) Systems** 16 (2008), p. 1210-1219
ISSN: 1063-8210
BibTeX: [Download](#)

- Angermeier J., Batzer U., Claus C., Majer M., Stechele W., Teich J.:
[Reconfigurable HW/SW Architecture of a Reconfigurable HW/SW Architecture of a Real-Time Driver Assistance System](#)
Fourth International Workshop on Applied Reconfigurable Computing (ARC) (London)
In: **Proceedings of the Fourth International Workshop on Applied Reconfigurable Computing**, Berlin Heidelberg: 2008
BibTeX: [Download](#)
- Angermeier J., Claus C., Stechele W., Teich J.:
[A comparison of embedded reconfigurable video-processing architectures](#)
International Conference on Field-Programmable Logic and Applications (FPL 08) (Heidelberg, 8. September 2008 - 10. September 2008)
In: **Proceedings of International Conference on Field-Programmable Logic and Applications**, New York: 2008
DOI: [10.1109/FPL.2008.4630015](#)
URL: <http://www.kip.uni-heidelberg.de/fpl08/titel/index.php>
BibTeX: [Download](#)
- Angermeier J., Hanke S., Majer M., Teich J., Wildermann S.:
[Co-Design Architecture and Implementation for Point-Based Rendering on FPGAs](#)
Proc. 19th IEEE/IFIP International Symposium on Rapid System Prototyping (RSP) (Monterey, 2. Juni 2008 - 5. Juni 2008)
In: **Proc. 19th IEEE/IFIP International Symposium on Rapid System Prototyping 2008**
DOI: [10.1109/RSP.2008.23](#)
BibTeX: [Download](#)
- Angermeier J., Teich J.:
[Heuristics for Scheduling Reconfigurable Devices with Consideration of Reconfiguration Overheads](#)
15th Reconfigurable Architectures Workshop (RAW 2008) (Miami, Florida, 14. April 2008 - 18. April 2008)
In: **Proceedings 15th Reconfigurable Architectures Workshop**, New York: 2008

DOI: [10.1109/IPDPS.2008.4536540](https://doi.org/10.1109/IPDPS.2008.4536540)

BibTeX: [Download](#)

- Beckhoff C., Koch D., Teich J.:

[ReCoBus-Builder - A Novel Tool and Technique to Build Statically and Dynamically Reconfigurable Systems for FPGAs](#)

International Conference on Field-Programmable Logic and Applications (FPL 08) (Heidelberg, 8. September 2008 - 10. September 2008)

In: **Proceedings of International Conference on Field-Programmable Logic and Applications**, New York: 2008

DOI: [10.1109/FPL.2008.4629918](https://doi.org/10.1109/FPL.2008.4629918)

BibTeX: [Download](#)

- Brendle R., Streichert T., Koch D., Haubelt C., Teich J.:

[Dynamic reconfiguration of FlexRay schedules for response time reduction in asynchronous fault-tolerant networks](#)

21st International Conference on Architecture of Computing Systems, ARCS 2008 (Dresden, 25. Februar 2008 - 28. Februar 2008)

In: **Proceedings of the International Conference on Architecture of Computing Systems (ARCS 2008) 2008**

DOI: [10.1007/978-3-540-78153-0_10](https://doi.org/10.1007/978-3-540-78153-0_10)

BibTeX: [Download](#)

- Dorsch R., Haubelt C., Teich J.:

[Entdecke die Möglichkeiten](#)

In: **Design & Elektronik** (2008), p. 22-27

ISSN: 0933-8667

BibTeX: [Download](#)

- Dutta Hritam, Hannig Frank, Hartl Matthias, Kissler Dmitrij, Teich Jürgen:

[Domain-Specific Reconfigurable MPSoC-Systems - Challenges and Trends](#)

Friday Workshop Reconfigurable Hardware, Design, Automation and Test in Europe (Munich, Germany)

In: **Friday Workshop Reconfigurable Hardware, Design, Automation and Test in Europe**, New York: 2008

BibTeX: [Download](#)

- Dutta H., Hannig F., Ruckdeschel H., Teich J.:
[Quantitative Evaluation of Behavioral Synthesis Approaches for Reconfigurable Devices](#)
2nd HiPEAC Workshop on Reconfigurable Computing (Gothenburg)
In: **Proceedings of the 2nd HiPEAC Workshop on Reconfigurable Computing** 2008
BibTeX: [Download](#)
- [Falk J.](#), Keinert J., Haubelt C., Teich J., Bhattacharyya SS.:
[A Generalized Static Data Flow Clustering Algorithm for MPSoC Scheduling of Multimedia Applications](#)
8th ACM & IEEE international conference on Embedded software (EMSOFT'2008) (Atlanta, Georgia, 20. Oktober 2008 - 22. Oktober 2008)
In: **Proc. of the 8th ACM & IEEE international conference on Embedded software (EMSOFT'2008)** 2008
BibTeX: [Download](#)
- Fekete SP., Kamphans T., Schweer N., Tessars C., Van Der Veen JC., Angermeyer J., Koch D., Teich J.:
[No-Break Dynamic Defragmentation of Reconfigurable Devices](#)
International Conference on Field-Programmable Logic and Applications (FPL 08) (Heidelberg, 8. September 2008 - 10. September 2008)
In: **Proceedings of International Conference on Field-Programmable Logic and Applications**, New York: 2008
DOI: [10.1109/FPL.2008.4629917](#)
BibTeX: [Download](#)
- Gladigau J., Blendinger F., Haubelt C., Teich J.:
[Symbolische Modellprüfung Aktor-orientierter High-level SystemC-Modelle mit Intervalldiagrammen](#)
11. GI/ITG/GMM-Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (Freiburg, 3. März 2008 - 5. März 2008)
BibTeX: [Download](#)
- Gladigau J., Haubelt C., Niemann B., Teich J.:
[Mapping Actor-Oriented Models to TLM Architectures](#)

Forum on specification and Design Languages 2007 (Barcelona, 18. September 2007 - 20. September 2007)

In: **Proceedings FDL'07, Forum on specification and Design Languages 2007** 2008

BibTeX: [Download](#)

- Gladigau J., Haubelt C., Teich J.:

[Symbolic quasi-static scheduling of actor-oriented SystemC models](#)

2008 Forum on Specification, Verification and Design Languages, FDL'08 (Stuttgart)

In: **Proceedings of Forum on specification & Design Languages 2008 (FDL08)** 2008

DOI: [10.1109/FDL.2008.4641412](https://doi.org/10.1109/FDL.2008.4641412)

BibTeX: [Download](#)

- Glaß M., Lukasiewicz M., Reimann F., Haubelt C., Teich J.:

[Symbolic reliability analysis and optimization of ECU networks](#)

Design, Automation and Test in Europe, DATE 2008 (Munich, 10. April 2008 - 14. April 2008)

In: **Proceedings of Design, Automation and Test in Europe (DATE 2008)** 2008

DOI: [10.1109/DATE.2008.4484679](https://doi.org/10.1109/DATE.2008.4484679)

BibTeX: [Download](#)

- Glaß M., Lukasiewicz M., Reimann F., Haubelt C., Teich J.:

[Symbolic reliability analysis of self-healing networked embedded systems](#)

27th International Conference on Computer Safety, Reliability, and Security, SAFECOMP 2008 (Newcastle upon Tyne, 22. September 2008 - 25. September 2008)

In: **Proceedings of the 27th International Conference on Computer Safety, Reliability and Security (SAFECOMP 2008)** 2008

DOI: [10.1007/978-3-540-87698-4_14](https://doi.org/10.1007/978-3-540-87698-4_14)

BibTeX: [Download](#)

- Glaß M., Lukasiewicz M., Teich J.:

[A Feasibility-Preserving Crossover and Mutation Operator for Constrained Combinatorial Problems](#)

*10th International Conference on Parallel Problem Solving from Nature (PPSN08)
(Dortmund, 13. September 2008 - 17. September 2008)*

In: **Proceedings of the 10th International Conference on Parallel Problem Solving from Nature**, Berlin, Heidelberg: 2008

DOI: [10.1007/978-3-540-87700-4](https://doi.org/10.1007/978-3-540-87700-4)

URL: <http://ls11-www.cs.uni-dortmund.de/ppsn/ppsn10/>

BibTeX: [Download](#)

- Glaß M., Lukasiwycz M., [Wanka R.](#), Haubelt C., Teich J.:
[Multi-objective routing and topology optimization in networked embedded systems](#)
Int. Conf. on Embedded Computer Systems: Architectures, Modeling, and Simulation (IC-SAMOS) (Samos)
In: **Proc. 8th Int. Conf. on Embedded Computer Systems: Architectures, Modeling, and Simulation (IC-SAMOS) 2008**
DOI: [10.1109/ICSAMOS.2008.4664849](https://doi.org/10.1109/ICSAMOS.2008.4664849)
BibTeX: [Download](#)
- Hannig F., Ruckdeschel H., Dutta H., Teich J.:
[PARO: Synthesis of Hardware Accelerators for Multi-Dimensional Dataflow-Intensive Applications](#)
*Fourth International Workshop on Applied Reconfigurable Computing (ARC)
(London, 26. März 2008 - 28. März 2008)*
In: **Proceedings of the Fourth International Workshop on Applied Reconfigurable Computing**, Berlin Heidelberg: 2008
DOI: [10.1007/978-3-540-78610-8_30](https://doi.org/10.1007/978-3-540-78610-8_30)
BibTeX: [Download](#)
- Hannig F., Ruckdeschel H., Teich J.:
[The PAULA Language for Designing Multi-Dimensional Dataflow-Intensive Applications](#)
GI/ITG/GMM-Workshop -- Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (Freiburg, 3. März 2008 - 5. März 2008)
In: **Proceedings of the GI/ITG/GMM-Workshop -- Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und**

Systemen 2008

BibTeX: [Download](#)

- Haubelt C., Koch D., Teich J.:

[Efficient reconfigurable on-chip buses for fpgas](#)

16th IEEE Symposium on Field-Programmable Custom Computing Machines, FCCM'08 (Palo Alto, California)

In: **Proceedings 16th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM 2008) 2008**

DOI: [10.1109/FCCM.2008.33](https://doi.org/10.1109/FCCM.2008.33)

BibTeX: [Download](#)

- Keinert J., Haubelt C., Teich J.:

[Automatic Synthesis of Design Alternatives for Fast Stream-Based Out-of-Order Communication](#)

2008 IFIP/IEEE WG 10.5 International Conference on Very Large Scale Integration, (VLSI-SoC 2008) (Rhodes Island, 13. Oktober 2008 - 15. Oktober 2008)

In: **Proceedings of the 2008 IFIP/IEEE WG 10.5 International Conference on Very Large Scale Integration, (VLSI-SoC 2008) 2008**

BibTeX: [Download](#)

- Keinert J., Haubelt C., Teich J.:

[Synthesis of multi-dimensional high-speed FIFOs for out-of-order communication](#)

21st International Conference on Architecture of Computing Systems, ARCS 2008 (Dresden, 25. Februar 2008 - 28. Februar 2008)

In: **Proceedings of the International Conference on Architecture of Computing Systems (ARCS 2008) 2008**

DOI: [10.1007/978-3-540-78153-0_11](https://doi.org/10.1007/978-3-540-78153-0_11)

BibTeX: [Download](#)

- Kissler D., Strawetz A., Hannig F., Teich J.:

[Power-efficient Reconfiguration Control in Coarse-Grained Dynamically Reconfigurable Architectures](#)

18th International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS) (Lisbon, 10. September 2008 - 12. September 2008)

In: **Proceedings of the 18th International Workshop on Power and Timing**

Modeling, Optimization and Simulation (PATMOS) 2008

BibTeX: [Download](#)

- Kupriyanov O., Hannig F., Kissler D., Teich J.:
[MAML: An ADL for Designing Single and Multiprocessor Architectures](#)
In: Prabhat Mishra and Nikil Dutt (ed.): **Processor Description Languages**,
Elsevier Inc., 2008, p. 295-327 (Systems on Silicon Series)
ISBN: 9780123742872
DOI: [10.1016/B978-012374287-2.50015-X](https://doi.org/10.1016/B978-012374287-2.50015-X)
BibTeX: [Download](#)
- Lukasiwycz M., Glaß M., Haubelt C., Teich J.:
[A feasibility-preserving local search operator for constrained discrete optimization problems](#)
2008 IEEE Congress on Evolutionary Computation, CEC 2008 (Hong Kong)
In: **Proceedings of the 2008 IEEE Congress on Evolutionary Computation (CEC 2008)** 2008
DOI: [10.1109/CEC.2008.4631058](https://doi.org/10.1109/CEC.2008.4631058)
BibTeX: [Download](#)
- Lukasiwycz M., Glaß M., Haubelt C., Teich J.:
[Efficient symbolic multi-objective design space exploration](#)
2008 Asia and South Pacific Design Automation Conference, ASP-DAC (Seoul)
DOI: [10.1109/ASPDAC.2008.4484040](https://doi.org/10.1109/ASPDAC.2008.4484040)
BibTeX: [Download](#)
- Lukasiwycz M., Glaß M., Haubelt C., Teich J., Regler R., Lang B.:
[Concurrent topology and routing optimization in automotive network integration](#)
45th Design Automation Conference, DAC (Anaheim, CA, 8. Juni 2008 - 13. Juni 2008)
In: **Proceedings of the 2008 ACM/EDAC/IEEE Design Automation Conference (DAC 2008)** 2008
DOI: [10.1109/DAC.2008.4555893](https://doi.org/10.1109/DAC.2008.4555893)
BibTeX: [Download](#)
- Reimann F., Glaß M., Lukasiwycz M., Keinert J., Haubelt C., Teich J.:
[Symbolic voter placement for dependability-aware system synthesis](#)

Embedded Systems Week 2008 - 6th IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis, CODES+ISSS 2008 (Atlanta, GA, 19. Oktober 2008 - 24. Oktober 2008)

In: **Proceedings of the 6th International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) 2008**

DOI: [10.1145/1450135.1450190](https://doi.org/10.1145/1450135.1450190)

BibTeX: [Download](#)

- Schaffer R., Merker R., Hannig F., Teich J.:

Utilization of all Levels of Parallelism in a Processor Array with Subword Parallelism

11th Euromicro Conference on Digital System Design (DSD) (Parma, 3. September 2008 - 5. September 2008)

In: **Proceedings of the 11th Euromicro Conference on Digital System Design**, New York: 2008

DOI: [10.1109/DSD.2008.24](https://doi.org/10.1109/DSD.2008.24)

BibTeX: [Download](#)

- Schmid M., Ziener D., Teich J.:

Netlist-Level IP Protection by Watermarking for LUT-Based FPGAs

IEEE International Conference on Field-Programmable Technology (FPT) (Taipei, 7. Dezember 2008 - 10. Dezember 2008)

In: **Proceedings of IEEE International Conference on Field-Programmable Technology**, New York: 2008

DOI: [10.1109/FPT.2008.4762385](https://doi.org/10.1109/FPT.2008.4762385)

BibTeX: [Download](#)

- Streichert T., Glaß M., [Wanka R.](#), Haubelt C., Teich J.:

Topology-aware replica placement in fault-tolerant embedded networks

21st International Conference on Architecture of Computing Systems (ARCS) (Dresden, 25. Februar 2008 - 28. Februar 2008)

In: **Proc. 21st International Conference on Architecture of Computing Systems (ARCS) 2008**

DOI: [10.1007/978-3-540-78153-0_4](https://doi.org/10.1007/978-3-540-78153-0_4)

URL: <http://www12.cs.fau.de/people/rwanka/publications/SGWHT08.php>

BibTeX: [Download](#)

- Streichert T., Koch D., Haubelt C., Teich J.:
[Concepts for self-adaptive and self-healing networked embedded systems](#)
In: Rolf Würtz (ed.): **Organic Computing**, Springer, 2008, p. 241-260 (Springer Series Understanding Complex Systems)
ISBN: 9783540776567
DOI: [10.1007/978-3-540-77657-4_11](https://doi.org/10.1007/978-3-540-77657-4_11)
BibTeX: [Download](#)
- Streubühr M., Jäntschi M., Haubelt C., Teich J., Schneider A.:
[Semi-Automatic Generation of mixed Hardware-Software Prototypes from Simulink Models](#)
11. GI/ITG/GMM-Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (Freiburg, 3. März 2008 - 5. März 2008)
In: **11. GI/ITG/GMM-Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen 2008**
BibTeX: [Download](#)
- Teich J.:
[Foreword DFG SPP1148 session:](#)
2008 International Conference on Field Programmable Logic and Applications, FPL (Heidelberg)
DOI: [10.1109/FPL.2008.4629962](https://doi.org/10.1109/FPL.2008.4629962)
BibTeX: [Download](#)
- Teich J.:
[Invasive Algorithms and Architectures](#)
In: **it - Information Technology** 50 (2008), p. 300-310
ISSN: 1611-2776
BibTeX: [Download](#)
- Teich J., Platzner M.:
[Proceedings - 2008 International Conference on Field Programmable Logic and Applications, FPL: Preface](#)
2008 International Conference on Field Programmable Logic and Applications, FPL (Heidelberg)

DOI: [10.1109/FPL.2008.4629893](https://doi.org/10.1109/FPL.2008.4629893)

BibTeX: [Download](#)

- Teich J., Wildermann S.:

[A Sequential Learning Resource Allocation Network for Image Processing Applications](#)

8th International Conference on Hybrid Intelligent Systems (Barcelona, 10. September 2008 - 12. September 2008)

In: **Proceedings of the 8th International Conference on Hybrid Intelligent Systems**, New York: 2008

DOI: [10.1109/HIS.2008.101](https://doi.org/10.1109/HIS.2008.101)

BibTeX: [Download](#)

- Wildermann S., Teich J.:

[3D Person Tracking with a Color-Based Particle Filter](#)

RobVis'2008 (Auckland, 18. Februar 2008 - 20. Februar 2008)

In: **Robot Vision**, Berlin: 2008

DOI: [10.1007/978-3-540-78157-8_25](https://doi.org/10.1007/978-3-540-78157-8_25)

BibTeX: [Download](#)

- Wildermann S., Teich J.:

[Theoretical Analysis of Fair Bandwidth Sharing in Priority-based Medium Access](#)

(2008)

BibTeX: [Download](#)

(Techreport)

- Wolinski C., Kuchcinski K., Teich J., Hannig F.:

[Area and Reconfiguration Time Minimization of the Communication Network in Regular 2D Reconfigurable Architectures](#)

International Conference on Field Programmable Logic and Applications (FPL) (Heidelberg, 8. September 2008 - 10. September 2008)

In: **Proceedings of the International Conference on Field Programmable Logic and Applications**, New York: 2008

DOI: [10.1109/FPL.2008.4629969](https://doi.org/10.1109/FPL.2008.4629969)

BibTeX: [Download](#)

- Wolinski C., Kuchcinski K., Teich J., Hannig F.:
[Communication Network Reconfiguration Overhead Optimization in Programmable Processor Array Architectures](#)
11th Euromicro Conference on Digital System Design (DSD) (Parma, 3. September 2008 - 5. September 2008)
In: **Proceedings of the 11th Euromicro Conference on Digital System Design**, New York: 2008
DOI: [10.1109/DSD.2008.1](https://doi.org/10.1109/DSD.2008.1)
BibTeX: [Download](#)
- Wolinski C., Kuchcinski K., Teich J., Hannig F.:
[Optimization of Routing and Reconfiguration Overhead in Programmable Processor Array Architectures](#)
16th IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM) (Palo Alto, CA, 14. April 2008 - 15. April 2008)
In: **Proceedings of the 16th IEEE Symposium on Field-Programmable Custom Computing Machines 2008**
DOI: [10.1109/FCCM.2008.16](https://doi.org/10.1109/FCCM.2008.16)
BibTeX: [Download](#)
- Zebelein C., [Falk J.](#), Haubelt C., Teich J.:
[Classification of general data flow actors into known models of computation](#)
6th ACM and IEEE International Conference on Formal Methods and Models for Co-Design, MEMOCODE'08 (Anaheim, CA, 5. Juli 2008 - 7. Juli 2008)
In: **Proc. of the Sixth ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE 2008) 2008**
DOI: [10.1109/MEMCOD.2008.4547699](https://doi.org/10.1109/MEMCOD.2008.4547699)
BibTeX: [Download](#)
- Ziener D., Teich J.:
[Concepts for Autonomous Control Flow Checking for Embedded CPUs](#)
5th International Conference on Autonomic and Trusted Computing (ATC-08) (Oslo, 23. Juni 2008 - 25. Juni 2008)
In: **Proceedings of the 5th International Conference on Autonomic and Trusted Computing (ATC-08)**, Berlin, Heidelberg: 2008

DOI: [10.1007/978-3-540-69295-9_20](https://doi.org/10.1007/978-3-540-69295-9_20)

BibTeX: [Download](#)

- Ziener D., Teich J.:

[Power Signature Watermarking of IP Cores for FPGAs](#)

In: **Journal of Signal Processing Systems For Signal Image and Video Technology** 51 (2008), p. 123-136

ISSN: 1939-8018

DOI: [10.1007/s11265-007-0136-8](https://doi.org/10.1007/s11265-007-0136-8)

BibTeX: [Download](#)

2007

- Ahmadinia A., Bobda C., Fekete SP., Teich J., Van Der Veen JC.:

[Optimal free-space management and routing-conscious dynamic placement for reconfigurable devices](#)

In: **IEEE Transactions on Computers** 56 (2007), p. 673-680

ISSN: 0018-9340

DOI: [10.1109/TC.2007.1028](https://doi.org/10.1109/TC.2007.1028)

BibTeX: [Download](#)

- Angermeier J., Fekete SP., Göhringer D., Majer M., Teich J., Van Der Veen JC.:
[Scheduling and communication-aware mapping of HW-SW modules for dynamically and partially reconfigurable SoC architectures](#)

ARCS '07 - 20th International Conference on Architecture of Computing Systems (Zurich)

In: **Proc. of the 20th International Conference on Architecture of Computing Systems**, Berlin: 2007

BibTeX: [Download](#)

- Angermeier J., Göhringer D., Majer M., Teich J., Fekete SP., Van Der Veen JC.:
[The Erlangen Slot Machine: A Platform for Interdisciplinary Research in Reconfigurable Computing](#)

In: **it - Information Technology** 49 (2007), p. 143-148

ISSN: 1611-2776

BibTeX: [Download](#)

- Bergmann N., Platzner M., Teich J.:
[Dynamically Reconfigurable Architectures](#)
In: **EURASIP Journal on Embedded Systems 2007** (2007), p. Article ID 28405,
2 pages
ISSN: 1687-3955
BibTeX: [Download](#)
- Bobda C., Majer M., Teich J., Ahmadinia A.:
[The Erlangen Slot Machine: A Dynamically Reconfigurable FPGA-Based Computer](#)
In: **Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology 47** (2007), p. 15-31
ISSN: 1387-5485
BibTeX: [Download](#)
- Dutta H., Hannig F., Kupriyanov O., Kissler D., Teich J., Schaffer R., Siegel S., Merker R., Pottier B.:
[Massively Parallel Processor Architectures: A Co-design Approach](#)
3rd International Workshop on Reconfigurable Communication Centric System-on-Chips (ReCoSoC) (Montpellier, 18. Juni 2007 - 20. Juni 2007)
In: **Proceedings of the 3rd International Workshop on Reconfigurable Communication Centric System-on-Chips (ReCoSoC) 2007**
BibTeX: [Download](#)
- Dutta H., Hannig F., Ruckdeschel H., Teich J.:
[Efficient Control Generation for Mapping Nested Loop Programs onto Processor Arrays](#)
In: **Journal of Systems Architecture 53** (2007), p. 300-309
ISSN: 1383-7621
DOI: [10.1016/j.sysarc.2006.10.009](https://doi.org/10.1016/j.sysarc.2006.10.009)
BibTeX: [Download](#)
- [Falk J.](#), Haubelt C., Teich J.:
[Task Graph Clustering with Internal State](#)
(2007)
BibTeX: [Download](#)
(Techreport)

- Glaß M., Lukasiwycz M., Haubelt C., Streichert T., Teich J.:
[Synthese zuverlässiger und flexibler Systeme](#)
Zuverlässigkeit und Entwurf (ZuD 2007) (Munich, 26. März 2007 - 28. März 2007)
In: **Proceedings of Zuverlässigkeit und Entwurf (ZuD 2007) 2007**
BibTeX: [Download](#)
- Haubelt C., [Falk J.](#), Keinert J., Schlichter T., Streubühr M., Deyhle A., Hadert A., Teich J.:
[A SystemC-based Design Methodology for Digital Signal Processing Systems](#)
In: **EURASIP Journal on Embedded Systems 2007 (2007)**, p. Article ID 47580, 22 pages
ISSN: 1687-3955
DOI: [10.1155/2007/47580](#)
BibTeX: [Download](#)
- Haubelt C., Teich J.:
[Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen](#)
Aachen: Shaker Verlag, 2007
BibTeX: [Download](#)
- Keinert J., [Falk J.](#), Haubelt C., Teich J.:
[Actor-oriented modeling and simulation of sliding window image processing algorithms](#)
2007 5th Workshop on Embedded Systems for Real-Time Multimedia, ESTIMedia 2007 (Salzburg, 4. Oktober 2007 - 5. Oktober 2007)
In: **Proceedings of the 2007 IEEE/ACM/IFIP Workshop of Embedded Systems for Real-Time Multimedia (ESTIMEDIA 2007) 2007**
DOI: [10.1109/ESTMED.2007.4375815](#)
BibTeX: [Download](#)
- Keinert J., Haubelt C., Teich J.:
[Simulative buffer analysis of local image processing algorithms described by windowed synchronous data flow](#)
2007 International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation, IC-SAMOS 2007 (Samos, 16. Juli 2007 - 19. Juli 2007)

In: **Proceedings of the International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation, Acoustics, Speech, and Signal Processing (IC-SAMOS VII) 2007**

DOI: [10.1109/ICSAMOS.2007.4285747](https://doi.org/10.1109/ICSAMOS.2007.4285747)

BibTeX: [Download](#)

- Kissler D., Hannig F., Teich J.:

[Schwach-programmiert macht stark](#)

In: **Design & Elektronik** (2007), p. 34-39

ISSN: 0933-8667

BibTeX: [Download](#)

- Koch D., Beckhoff C., Teich J.:

[Bitstream Decompression for High Speed FPGA Configuration from Slow Memories](#)

IEEE International Conference on Field-Programmable Technology 2007

(ICFPT'07) (Kokurakita, Kitakyushu, 12. Dezember 2007 - 14. Dezember 2007)

In: **Proc. of the IEEE International Conference on Field-Programmable Technology 2007**, New York: 2007

DOI: [10.1109/FPT.2007.4439245](https://doi.org/10.1109/FPT.2007.4439245)

BibTeX: [Download](#)

- Koch D., Haubelt C., Streichert T., Teich J.:

[Modeling and synthesis of hardware-software morphing](#)

2007 IEEE International Symposium on Circuits and Systems, ISCAS 2007 (New Orleans, LA)

In: **Proceedings of the International Symposium on Circuits and Systems (ISCAS 2007) 2007**

URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=34548813114&origin=inward>

BibTeX: [Download](#)

- Koch D., Haubelt C., Teich J.:

[Efficient hardware checkpointing: Concepts, overhead analysis, and implementation](#)

FPGA 2007: Fifteenth ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (Monterey, CA, 18. Februar 2007 - 20. Februar 2007)

In: **Proceedings of the 15th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2007)** 2007

DOI: [10.1145/1216919.1216950](https://doi.org/10.1145/1216919.1216950)

BibTeX: [Download](#)

- Kupriyanov O., Hannig F., Kissler D., Teich J., Lallet J., Sentieys O., Pillement S.:
[Modeling of interconnection networks in massively parallel processor architectures](#)

20th International Conference on Architecture of Computing Systems, ARCS 2007 (Zurich, 12. März 2007 - 15. März 2007)

In: **Proceedings of the 20th International Conference on Architecture of Computing Systems (ARCS 2007)** 2007

URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=37249015485&origin=inward>

BibTeX: [Download](#)

- Kupriyanov O., Kissler D., Hannig F., Teich J.:
[Efficient event-driven simulation of parallel processor architectures](#)
10th International Workshop on Software and Compilers for Embedded Systems, SCOPES 2007 (Nice)

In: **Proceedings of the 10th International Workshop on Software and Compilers for Embedded Systems (SCOPES)** 2007

DOI: [10.1145/1269843.1269854](https://doi.org/10.1145/1269843.1269854)

BibTeX: [Download](#)

- Lukasiewicz M., Glaß M., Haubelt C., Teich J.:
[SAT-decoding in evolutionary algorithms for discrete constrained optimization problems](#)

2007 IEEE Congress on Evolutionary Computation, CEC 2007 (Singapore, 25. September 2007 - 28. September 2007)

In: **In Proceedings of the 2007 IEEE Congress on Evolutionary Computation (CEC 2007)** 2007

DOI: [10.1109/CEC.2007.4424570](https://doi.org/10.1109/CEC.2007.4424570)

BibTeX: [Download](#)

- Lukasiewicz M., Glaß M., Haubelt C., Teich J.:
[Solving multi-objective Pseudo-Boolean problems](#)

10th International Conference on Theory and Applications of Satisfiability Testing, SAT 2007 (Lisbon, 28. Mai 2007 - 31. Mai 2007)

In: **Proceedings of Tenth International Conference on Theory and Applications of Satisfiability Testing (SAT 2007) 2007**

URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=38049113235&origin=inward>

BibTeX: [Download](#)

- Lukasiwycz M., Glaß M., Haubelt C., Teich J.:
[Symbolic archive representation for a fast nondominance test](#)
4th International Conference on Evolutionary Multi-Criterion Optimization, EMO 2007 (Matsushima, 5. März 2007 - 8. März 2007)
URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=37249008208&origin=inward>
BibTeX: [Download](#)
- Niemann B., Haubelt C., Uribe M., Teich J.:
[Formalizing TLM with Communicating State Machines](#)
In: Sorin A. Huss (ed.): **Advances in Design and Specification Languages for Embedded Systems**, Springer, 2007, p. 225-242
BibTeX: [Download](#)
- Stechele W., Bringmann O., Ernst R., Herkersdorf A., Hojenski K., Janacik P., Rammig F., Teich J., Wehn N., Zeppenfeld J., Ziener D.:
[Autonomic MPSoCs for Reliable Systems](#)
Zuverlässigkeit und Entwurf (ZuD) (Munich)
In: **Proceedings of Zuverlässigkeit und Entwurf (ZuD 2007) 2007**
BibTeX: [Download](#)
- Stechele W., Bringmann O., Ernst R., Herkersdorf A., Hojenski K., Janacik P., Rammig F., Teich J., Wehn N., Zeppenfeld J., Ziener D.:
[Concepts for Autonomic Integrated Systems](#)
edaWorkshop07 (Hannover)
In: **Proceedings of edaWorkshop07**, Berlin: 2007
BibTeX: [Download](#)
- Streichert T., Glaß M., Haubelt C., Teich J.:
[Design space exploration of reliable networked embedded systems](#)

In: **Journal of Systems Architecture** 53 (2007), p. 751-763

ISSN: 1383-7621

DOI: [10.1016/j.sysarc.2007.01.005](https://doi.org/10.1016/j.sysarc.2007.01.005)

BibTeX: [Download](#)

- Streichert T., Strengert C., Koch D., Teich J., Haubelt C.:
[Communication Aware Optimization of the Task Binding in Hardware/Software Reconfigurable Networks](#)

In: **Journal of Integrated Circuits and Systems** (2007), p. 29-36

ISSN: 1807-1953

BibTeX: [Download](#)

- Streubühr M., Riedel C., Haubelt C., Teich J.:
[System Level Modeling and Performance Simulation for Dynamic Reconfigurable Computing Systems in SystemC](#)

10. Workshop "Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen" (Erlangen, 5. März 2007 - 7. März 2007)

In: **Proceedings of 10. Workshop "Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen" 2007**

BibTeX: [Download](#)

- Teich J.:
[Reconfigurable Computing Systems](#)

In: **it - Information Technology** 49 (2007), p. 139-142

ISSN: 1611-2776

BibTeX: [Download](#)

- Glaß M., Lukaszewicz M., Streichert T., Haubelt C., Teich J.:
[Reliability-aware system synthesis](#)

2007 Design, Automation and Test in Europe Conference and Exhibition (Nice Acropolis, 16. April 2007 - 20. April 2007)

In: **Proceedings of Design, Automation and Test in Europe (DATE 2007) 2007**

DOI: [10.1109/DATE.2007.364626](https://doi.org/10.1109/DATE.2007.364626)

BibTeX: [Download](#)

- Teich J., Hannig F., Ruckdeschel H., Dutta H., Kissler D., Stravet A.:
[**A Unified Retargetable Design Methodology for Dedicated and Re-Programmable Multiprocessor Arrays: Case Study and Quantitative Evaluation**](#)
International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA) (Las Vegas, NV, 25. Juni 2007 - 28. Juni 2007)
In: **Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA) 2007**
BibTeX: [Download](#)
- Teich J., Haubelt C.:
[**Digitale Hardware/Software-Systeme: Synthese und Optimierung**](#)
Berlin: Springer, 2007
ISBN: 978-3-540-46822-6
URL: <http://www.springer.com/computer/hardware/book/978-3-540-46822-6>
BibTeX: [Download](#)

2006

- Ahmadinia A., Bobda C., Teich J.:
[**Online Placement for Dynamically Reconfigurable Devices**](#)
In: **EURASIP Journal on Embedded Systems** 1 (2006), p. 165-178
ISSN: 1687-3955
BibTeX: [Download](#)
- Becker J., Teich J., Athanas P., Brebner G.:
[**Dynamically Reconfigurable Architectures**](#)
2006
(Proceedings of the Dagstuhl Seminar N° 06141)
BibTeX: [Download](#)
- Bhattacharyya SS., Teich J.:
[**Analysis of Dataflow Programs with Interval-limited Data-rates**](#)
In: **Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology** Vol. 43, Nos. 2-3 (2006), p. 247-258
ISSN: 1387-5485
DOI: [10.1007/s11265-006-7274-2](https://doi.org/10.1007/s11265-006-7274-2)
BibTeX: [Download](#)

- Dutta H., Hannig F., Heigl B., Hornegger H., Teich J.:
[**A Design Methodology for Hardware Acceleration of Adaptive Filter Algorithms in Image Processing**](#)
IEEE 17th International Conference on Application-specific Systems, Architectures, and Processors (ASAP) (Steamboat Springs, CO, 11. September 2006 - 13. September 2006)
In: **Proceedings of IEEE 17th International Conference on Application-specific Systems, Architectures, and Processors 2006**
DOI: [10.1109/ASAP.2006.4](https://doi.org/10.1109/ASAP.2006.4)
BibTeX: [Download](#)
- Dutta H., Hannig F., Teich J.:
[**A Formal Methodology for Hierarchical Partitioning of Piecewise Linear Algorithms**](#)
In: **Technical Report 04-2006**, 2006
BibTeX: [Download](#)
(Techreport)
- Dutta H., Hannig F., Teich J.:
[**Controller Synthesis for Mapping Partitioned Programs on Array Architectures**](#)
19th International Conference on Architecture of Computing Systems (ARCS) (Frankfurt am Main, 13. März 2006 - 16. März 2006)
In: **Proceedings of the 19th International Conference on Architecture of Computing Systems**, Berlin, Heidelberg, New York: 2006
DOI: [10.1007/11682127_13](https://doi.org/10.1007/11682127_13)
BibTeX: [Download](#)
- Dutta H., Hannig F., Teich J.:
[**Hierarchical Partitioning for Piecewise Linear Algorithms**](#)
5th International Conference on Parallel Computing in Electrical Engineering (PARELEC) (Bialystok, 13. September 2006 - 17. September 2006)
In: **Proceedings of the 5th International Conference on Parallel Computing in Electrical Engineering 2006**
DOI: [10.1109/PARELEC.2006.43](https://doi.org/10.1109/PARELEC.2006.43)
BibTeX: [Download](#)

- Dutta H., Hannig F., Teich J.:
[Mapping a Class of Dependence Algorithms to Coarse-grained Reconfigurable Arrays: Architectural Parameters and Methodology](#)
In: **International Journal of Embedded Systems** 2 (2006), p. 114-127
ISSN: 1741-1068
BibTeX: [Download](#)
- Dutta H., Hannig F., Teich J.:
[Mapping of Nested Loop Programs onto Massively Parallel Processor Arrays with Memory and I/O Constraints](#)
6th International Heinz Nixdorf Symposium, New Trends in Parallel & Distributed Computing (Paderborn, 17. Januar 2006 - 18. Januar 2006)
In: **Proceedings of the 6th International Heinz Nixdorf Symposium, New Trends in Parallel & Distributed Computing**, Paderborn, Germany: 2006
BibTeX: [Download](#)
- [Falk J.](#), Haubelt C., Teich J.:
[Efficient Representation and Simulation of Model-Based Designs in SystemC](#)
FDL'06, Forum on Design Languages 2006 (Darmstadt, 29. September 2006 - 22. September 2006)
In: **Proceedings FDL'06, Forum on Design Languages 2006** 2006
BibTeX: [Download](#)
- Fekete SP., Van Der Veen JC., Majer M., Teich J.:
[Minimizing communication cost for reconfigurable slot modules](#)
16th International Conference on Field Programmable Logic and Applications (FPL06) (Madrid, 28. August 2006 - 30. August 2006)
In: **Proceedings of 16th International Conference on Field Programmable Logic and Applications** 2006
DOI: [10.1109/FPL.2006.311263](#)
BibTeX: [Download](#)
- Göhringer D., Majer M., Teich J.:
[Bridging the Gap between Relocation and Available Technology: The Erlangen Slot Machine](#)
Dynamically Reconfigurable Architectures (Dagstuhl)

In: **Proceedings of the Dagstuhl Seminar N° 06141 on Dynamically Reconfigurable Architectures**, Dagstuhl, Germany: 2006

URL: <http://drops.dagstuhl.de/opus/volltexte/2006/736>

BibTeX: [Download](#)

- Hannig F., Dutta H., Teich J.:

[Mapping a Class of Dependence Algorithms to Coarse-grained Reconfigurable Arrays -- Architectural Parameters and Methodology](#)

In: **International Journal of Embedded Systems** 2 (2006), p. 114-127

ISSN: 1741-1068

DOI: [10.1504/IJES.2006.010170](https://doi.org/10.1504/IJES.2006.010170)

BibTeX: [Download](#)

- Hannig F., Merker R., Siegel S., Teich J.:

[Communication-conscious Mapping of Regular Nested Loop Programs onto Massively Parallel Processor Arrays](#)

18th International Conference on Parallel and Distributed Computing and Systems (PDCS) (Dallas, TX, 13. November 2006 - 15. November 2006)

In: **Proceedings of the 18th International Conference on Parallel and Distributed Computing and Systems** 2006

BibTeX: [Download](#)

- Haubelt C., Schlichter T., Teich J.:

[Improving Automatic Design Space Exploration by Integrating Symbolic Techniques into Multi-Objective Evolutionary Algorithms](#)

In: **International Journal of Computational Intelligence Research** 2 (2006), p. 239-254

ISSN: 0973-1873

BibTeX: [Download](#)

- Keinert J., Haubelt C., Teich J.:

[Modeling and analysis of windowed synchronous algorithms](#)

2006 IEEE International Conference on Acoustics, Speech and Signal Processing, ICASSP 2006 (Toulouse, 14. Mai 2006 - 19. Mai 2006)

In: **Proceedings of the 31st International Conference on Acoustics, Speech, and Signal Processing (ICASSP2006)** 2006

URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=33947613533&origin=inward>

BibTeX: [Download](#)

- Kissler D., Hannig F., Kupriyanov O., Teich J.:
[A Dynamically Reconfigurable Weakly Programmable Processor Array Architecture Template](#)
2nd International Workshop on Reconfigurable Communication-Centric System-on-Chips (ReCoSoC) (, 3. Juli 2006 - 5. Juli 2006)
In: **Proceedings of the 2nd International Workshop on Reconfigurable Communication-Centric System-on-Chips (ReCoSoC) 2006**
BibTeX: [Download](#)
- Kissler D., Hannig F., Kupriyanov O., Teich J.:
[Hardware cost analysis for weakly programmable processor arrays](#)
2006 International Symposium on System-on-Chip, SOC (Tampere, 14. November 2006 - 16. November 2006)
In: **Proceedings of the International Symposium on System-on-Chip (SoC) 2006**
DOI: [10.1109/ISSOC.2006.321996](https://doi.org/10.1109/ISSOC.2006.321996)
BibTeX: [Download](#)
- Kissler D., Kupriyanov O., Hannig F., Koch D., Teich J.:
[A Generic Framework for Rapid Prototyping of System-on-Chip Designs](#)
International Conference on Computer Design (CDES) (Las Vegas, NV)
In: **Proceedings of the International Conference on Computer Design (CDES) 2006**
BibTeX: [Download](#)
- Kissler D., Kupriyanov O., Hannig F., Teich J.:
[A highly parameterizable parallel processor array architecture](#)
2006 IEEE International Conference on Field Programmable Technology, FPT 2006 (Bangkok, 13. Dezember 2006 - 15. Dezember 2006)
In: **Proceedings of the IEEE International Conference on Field Programmable Technology (FPT 2006) 2006**
DOI: [10.1109/FPT.2006.270293](https://doi.org/10.1109/FPT.2006.270293)
BibTeX: [Download](#)

- Koch D., Streichert T., Dittrich S., Strengert C., Haubelt C., Teich J.:
[An operating system infrastructure for fault-tolerant reconfigurable networks](#)
19th International Conference on Architecture of Computing Systems, ARCS 2006 (Frankfurt, Main, 13. März 2006 - 16. März 2006)
In: **Proceedings of the 19th International Conference on Architecture of Computing Systems (ARCS 2006)** 2006
DOI: [10.1007/11682127_15](https://doi.org/10.1007/11682127_15)
BibTeX: [Download](#)
- Koch D., Streichert T., Teich J., Haubelt C.:
[Modeling and Design of Fault-Tolerant and Self-Adaptive Reconfigurable Networked Embedded Systems](#)
In: **EURASIP Journal on Embedded Systems** 2006 (2006), p. 1 - 15
ISSN: 1687-3955
DOI: [10.1155/ES/2006/42168](https://doi.org/10.1155/ES/2006/42168)
BibTeX: [Download](#)
- Koch D., Teich J., Körber M.:
[Searching RC5-Keys with Distributed Reconfigurable Computing](#)
International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA) (Las Vegas, 26. Juni 2006 - 29. Juni 2006)
In: **Proceedings of International Conference on Engineering of Reconfigurable Systems and Algorithms, USA: 2006**
BibTeX: [Download](#)
- Kupriyanov O., Hannig F., Kissler D., Schaffer R., Teich J.:
[MAML - An Architecture Description Language for Modeling and Simulation of Processor Array Architectures, Part I](#)
In: **Technical Report 03-2006**, 2006
BibTeX: [Download](#)
(Techreport)
- Kupriyanov O., Hannig F., Kissler D., Teich J., Lallet J., Sentieys O., Pillement S.:
[Modeling of Interconnection Networks in Massively Parallel Processor Architectures](#)
In: **Technical Report 05-2006**, 2006

BibTeX: [Download](#)

(Techreport)

- Kupriyanov O., Hannig F., Kissler D., Teich J., Schaffer R., Merker R.:
[An Architecture Description Language for Massively Parallel Processor Architectures](#)
9th ITG/GMM/GI Workshop, Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (Dresden, 20. Februar 2006 - 22. Februar 2006)
In: **Proceedings of the 9th ITG/GMM/GI Workshop, Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen 2006**
BibTeX: [Download](#)
- Majer M., Ahmadiania A., Bobda C., Teich J.:
[A Flexible Reconfiguration Manager for the Erlangen Slot Machine](#)
M. Majer, A. Ahmadiania, C. Bobda and J. Teich (Frankfurt/Main, 16. März 2003 - 16. März 2003)
In: **Proceedings of the Dynamically Reconfigurable Systems Workshop (DRS'2006) 2006**
BibTeX: [Download](#)
- Schlichter T., Lukaszewicz M., Haubelt C., Teich J.:
[Improving system level design space exploration by incorporating SAT-solvers into multi-objective evolutionary algorithms](#)
IEEE Computer Society Annual Symposium on Emerging VLSI Technologies and Architectures 2006 (Karlsruhe, 2. März 2006 - 3. März 2006)
In: **Proceedings of IEEE Computer Society Annual Symposium on VLSI. Karlsruhe 2006**
DOI: [10.1109/ISVLSI.2006.57](https://doi.org/10.1109/ISVLSI.2006.57)
BibTeX: [Download](#)
- Streichert T., Haubelt C., Teich J.:
[Multi-objective topology optimization for networked embedded systems](#)
2006 International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation, IC-SAMOS 2006 (Samos, 17. Juli 2006 - 20. Juli 2006)
In: **Proceedings of the International Conference on Embedded Computer**

Systems: Architectures, Modeling, and Simulation (IC-SAMOS 2006) 2006

DOI: [10.1109/ICSAMOS.2006.300814](https://doi.org/10.1109/ICSAMOS.2006.300814)

BibTeX: [Download](#)

- Streichert T., Strengert C., Haubelt C., Teich J.:
[Dynamic task binding for hardware/software reconfigurable networks](#)
SBCCI 2006 - 19th Symposium on Integrated Circuits and Systems Design (Ouro Preto)
In: **In Proceedings of SBCCI 2006** 2006
URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=33750914830&origin=inward>
BibTeX: [Download](#)
- Streubühr M., [Falk J.](#), Teich J., Haubelt C., Dorsch R., Schlipf T.:
[Task-accurate performance modeling in SystemC for real-time multi-processor architectures](#)
Design, Automation and Test in Europe, DATE'06 (Munich, 6. März 2006 - 10. März 2006)
In: **Proceedings of Design, Automation and Test in Europe (DATE 2006), IEEE Computer Society** 2006
URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=34047100936&origin=inward>
BibTeX: [Download](#)
- Teich J.:
[Are Current ESL Tools Meeting the Requirements of Advanced Embedded Systems?](#)
4th international conference on Hardware/software codesign and system synthesis (Seoul, 22. Oktober 2006 - 25. Oktober 2006)
In: **CODES ISSS '06: Proceedings of the 4th international conference on Hardware/software codesign and system synthesis**, New York, NY, USA: 2006
DOI: [10.1145/1176254.1176295](https://doi.org/10.1145/1176254.1176295)
BibTeX: [Download](#)
- Teich J.:
[Stochastic Timing Analysis of Communicating Tasks with Internal State](#)

- In: **Technical Report 02-2006**, 2006
BibTeX: [Download](#)
(Techreport)
- Teich J.:
[**Timing Analysis of Systems of Communicating Tasks with Internal State**](#)
In: **Technical Report 01-2006**, 2006
BibTeX: [Download](#)
(Techreport)
 - Teich J., Fekete SP., Köhler E.:
[**Higher-dimensional packing with order constraints**](#)
In: **SIAM Journal on Discrete Mathematics** (2006), p. 1056-1078
ISSN: 0895-4801
BibTeX: [Download](#)
 - Teich J., Kaxiras S., Plaks T., Flautner K.:
[**Topic 18: Embedded Parallel Systems**](#)
Euro-Par 2006 Parallel Processing (Dresden, 28. August 2006 - 1. September 2006)
In: **Proceedings of the 12th International Euro-Par Conference**, Berlin, Heidelberg, New York: 2006
DOI: [10.1007/11823285_124](https://doi.org/10.1007/11823285_124)
BibTeX: [Download](#)
 - Ziener D., Aßmus Stefan AS., Teich J.:
[**Identifying FPGA IP-Cores based on Lookup Table Content Analysis**](#)
16th International Conference on Field Programmable Logic and Applications (Madrid, 28. August 2006 - 30. August 2006)
In: **Proceedings of 16th International Conference on Field Programmable Logic and Applications 2006**
DOI: [10.1109/FPL.2006.311255](https://doi.org/10.1109/FPL.2006.311255)
BibTeX: [Download](#)
 - Ziener D., Teich J.:
[**FPGA Core Watermarking Based on Power Signature Analysis**](#)
IEEE International Conference on Field-Programmable Technology (FPT) (Bangkok, 13. Dezember 2006 - 15. Dezember 2006)

In: **Proceedings of IEEE International Conference on Field-Programmable Technology 2006**

DOI: [10.1109/FPT.2006.270313](https://doi.org/10.1109/FPT.2006.270313)

BibTeX: [Download](#)

2005

- Ahmadinia A., Bobda C., Ding J., Fekete SP., Majer M., Teich J., Van Der Veen JC.:

[**A Practical Approach for Circuit Routing on Dynamic Reconfigurable Devices**](#)

16th IEEE International Workshop on Rapid System Prototyping (RSP) (Montreal, 8. Juni 2005 - 10. Juni 2005)

In: **Proceedings of the 16th IEEE International Workshop on Rapid System Prototyping 2005**

BibTeX: [Download](#)

- Ahmadinia A., Bobda C., Ding J., Majer M., Teich J.:

[**Modular Video Streaming on a Reconfigurable Platform**](#)

IFIP VLSI-SoC (Perth)

In: **IFIP VLSI-SOC 2005 2005**

BibTeX: [Download](#)

- Ahmadinia A., Bobda C., Fekete SP., Haller T., Linarth AG., Majer M., Teich J., Van Der Veen JC.:

[**The Erlangen Slot Machine: A Highly Flexible FPGA-Based Reconfigurable Platform**](#)

13th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (Marriott at Napa Valley, California, 18. April 2005 - 20. April 2005)

In: **Proceedings of the 13th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'05) 2005**

DOI: [10.1109/FCCM.2005.63](https://doi.org/10.1109/FCCM.2005.63)

BibTeX: [Download](#)

- Ahmadinia A., Bobda C., Fekete SP., Hannig F., Majer M., Teich J., Van Der Veen JC.:

[**Defragmenting the Module Layout of a Partially Reconfigurable Device**](#)

International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA) (Las Vegas, NV, 27. Juni 2005 - 30. Juni 2005)

In: **Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms 2005**

BibTeX: [Download](#)

- Ahmadinia A., Bobda C., Fekete SP., Majer M., Teich J., Van Der Veen JC.:
[**DyNoC: A Dynamic Infrastructure for Communication in Dynamically Reconfigurable Devices**](#)

International Conference on Field-Programmable Logic and Applications (FPL) (Tampere, 24. August 2005 - 26. August 2005)

In: **Proceedings of the International Conference on Field-Programmable Logic and Applications 2005**

DOI: [10.1109/FPL.2005.1515715](https://doi.org/10.1109/FPL.2005.1515715)

BibTeX: [Download](#)

- Ahmadinia A., Bobda C., Haller T., Linarth AG., Majer M., Teich J.:
[**Increasing the Flexibility in FPGA-Based Reconfigurable Platforms: The Erlangen Slot Machine**](#)

IEEE Conference on Field-Programmable Technology (FPT) (Singapore, 11. Dezember 2005 - 14. Dezember 2005)

In: **IEEE 2005 Conference on Field-Programmable Technology 2005**

DOI: [10.1109/FPT.2005.1568522](https://doi.org/10.1109/FPT.2005.1568522)

BibTeX: [Download](#)

- Ahmadinia A., Bobda C., Majer M., Teich J.:

[**Packet Routing in Dynamically Changing Networks on Chip**](#)

12th Reconfigurable Architectures Workshop (RAW 2005) (Denver, 4. April 2005 - 5. April 2005)

In: 2005 (ed.): **Proceedings of the 12th Reconfigurable Architectures Workshop (RAW 2005) 2005**

BibTeX: [Download](#)

- Dinkel T., Haubelt C., Heinkel U., Schlichter T., Knäblein J., Schock T., Teich J.:
[**Comparison of Techniques for the Automatic Verification of ADeVA Specifications**](#)

Dresdener Arbeitstagung Schaltungs- und Systementwurf (DASS 2005) (Dresden, 13. April 2005 - 14. April 2005)

In: **Proc. Dresdener Arbeitstagung Schaltungs- und Systementwurf (DASS 2005) 2005**

BibTeX: [Download](#)

- Dinkel T., Haubelt C., Heinkel U., Schlichter T., Teich J.:

[Automatische Verification von ADeVA-Spezifikationen](#)

GI/ITG/GMM-Workshop 2005 (Munich, 6. April 2005 - 7. April 2005)

In: **Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen 2005**

BibTeX: [Download](#)

- Dutta H., Hannig F., Kupriyanov O., Teich J., Schaffer R., Siegel S., Merker R., Keryell R., Pottier B., Chillet D., Ménard D., Sentieys O.:

[Co-Design of Massively Parallel Embedded Processor Architectures](#)

First ReCoSoC Workshop (Montpellier)

In: **Proceedings of the first ReCoSoC Workshop 2005**

BibTeX: [Download](#)

- Dutta Hritam, Hannig Frank, Ruckdeschel Holger, Teich Jürgen:

[Automatic FIR Filter Generation for FPGAs](#)

Embedded Computer Systems: Architectures, Modeling, and Simulation. (Island of Samos, 18. Juli 2005 - 20. Juli 2005)

In: **In Proceedings of the 5th International Workshop on Embedded Computer Systems, Architectures, Modeling, and Simulation (SAMOS 2005)**, Berlin, Heidelberg, New York: 2005

BibTeX: [Download](#)

- Dutta H., Hannig F., Teich J.:

[Control Path Generation for Mapping Partitioned Dataflow-dominant Algorithms onto Array Architectures](#)

In: **Technical Report 03-2005**, 2005

BibTeX: [Download](#)

(Techreport)

- [Falk J.](#), Haubelt C., Teich J.:

[Representing Models of Computation in SystemC](#)

GI/ITG/GMM-Workshop 2005 (Munich, 6. April 2005 - 7. April 2005)

BibTeX: [Download](#)

- [Falk J.](#), Haubelt C., Teich J.:

[Syntax and execution behavior of SystemoC](#)

In: **Technical Report 04-2005**, 2005

BibTeX: [Download](#)

(Techreport)

- Hannig F., Teich J.:

[Output Serialization for FPGA-based and Coarse-grained Processor Arrays](#)

International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA) (Las Vegas, NV, 27. Juni 2005 - 30. Juni 2005)

In: **Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms 2005**

BibTeX: [Download](#)

- Haubelt C., Gamenik J., Teich J.:

[Initial Population Construction for Convergence Improvement of MOEAs](#)

In: Carlos A. Coello Coello, Arturo Hernández Aguirre, and Eckart Zitzler (ed.):

Evolutionary Multi-Criterion Optimization, Springer, 2005, p. 191-205 (Lecture Notes in Computer Science, Vol.3410)

BibTeX: [Download](#)

- Haubelt C., Jersak M., Richter K., Strehl K., Ziegenbein D., Ernst R., Teich J., Thiele L.:

[SPI-Workbench – Modellierung, Analyse und Optimierung eingebetteter Systeme](#)

In: Armin B. Cremers, Rainer Manthey, Peter Martini, and Volker Steinhage (ed.):

Proceedings of INFORMATIK 2005 - Informatik LIVE, 2005

BibTeX: [Download](#)

- Haubelt C., Otto S., Grabbe C., Teich J.:

[A system-level approach to hardware reconfigurable systems](#)

2005 Asia and South Pacific Design Automation Conference, ASP-DAC 2005 (Shanghai, 18. Januar 2005 - 21. Januar 2005)

In: **Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC'05) 2005**

URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=84861440285&origin=inward>

BibTeX: [Download](#)

- Helwig S., Haubelt C., Teich J.:

[Modeling and analysis of indirect communication in Particle Swarm Optimization](#)

2005 IEEE Congress on Evolutionary Computation, IEEE CEC 2005 (Edinburgh)

In: **Proceedings of the 2005 IEEE Congress on Evolutionary Computation 2005**

URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=27144530244&origin=inward>

BibTeX: [Download](#)

- Keinert J., Haubelt C., Teich J.:

[Windowed Synchronous Data Flow](#)

In: **Technical Report 02-2005**, 2005

BibTeX: [Download](#)

(Techreport)

- Mostaghim S., Teich J.:

[Quad-trees: A Data structure for storing Pareto-sets in Multi-objective Evolutionary Algorithms with Elitism](#)

In: Ajith Abraham and Lakhmi Jain and Robert Goldberg (ed.): **Evolutionary Multiobjective Optimization**, London: Springer, 2005, p. 81-104 (Advanced Information and Knowledge Processing)

BibTeX: [Download](#)

- Schlichter T., Hannig F., Haubelt C., Teich J.:

[Using symbolic feasibility tests during design space exploration of heterogeneous multi-processor systems](#)

IEEE 16th International Conference on Application-Specific Systems, Architectures, and Processors, ASAP 2005 (Samos)

In: **Proceedings of Application-specific Systems, Architectures and Processors (ASAP) 2005**

DOI: [10.1109/ASAP.2005.64](https://doi.org/10.1109/ASAP.2005.64)

BibTeX: [Download](#)

- Schlichter T., Haubelt C., Teich J.:
[Improving EA-based design space exploration by utilizing symbolic feasibility tests](#)
GECCO 2005 - Genetic and Evolutionary Computation Conference (Washington, D.C., 25. Juni 2005 - 29. Juni 2005)
In: Beyer H.G.; O'Reilly U.M.; Arnold D.; Banzhaf W.; Blum C.; Bonabeau E.W.; Cantu-Paz E.; Dasgupta D.; Deb K.; et al (ed.): **Proceedings of Genetic and Evolutionary Computation Conference (GECCO) 2005**
DOI: [10.1145/1068009.1068336](https://doi.org/10.1145/1068009.1068336)
BibTeX: [Download](#)
- Streichert T., Haubelt C., Teich J.:
[Distributed HW/SW-partitioning for embedded reconfigurable networks](#)
Design, Automation and Test in Europe, DATE '05 (Munich, 7. März 2005 - 11. März 2005)
In: **Proceedings of DATE 2005, Munich 2005**
DOI: [10.1109/DATE.2005.123](https://doi.org/10.1109/DATE.2005.123)
BibTeX: [Download](#)
- Streichert T., Haubelt C., Teich J.:
[Online hardware/software partitioning in networked embedded systems](#)
2005 Asia and South Pacific Design Automation Conference, ASP-DAC 2005 (Shanghai, 18. Januar 2005 - 21. Januar 2005)
In: **Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC'05) 2005**
URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=33745634653&origin=inward>
BibTeX: [Download](#)
- Streichert T., Haubelt C., Teich J.:
[Verteilte HW/SW-Partitionierung für fehlertolerante rekonfigurierbare Netzwerke](#)
17. ITG/GI/GMM Workshop für Testmethoden und Zuverlässigkeit und Fehlertoleranz von Schaltungen und Systemen (Innsbruck, 27. Februar 2005 - 1. März 2005)

In: **Proceedings of 17. ITG/GI/GMM Workshop für Testmethoden und Zuverlässigkeit und Fehlertoleranz von Schaltungen und Systemen 2005**

BibTeX: [Download](#)

- Ziener D., Teich J.:

[Evaluation of Watermarking methods for FPGA-based IP-cores](#)

In: **Technical Report 01-2005**, 2005

BibTeX: [Download](#)

(Techreport)

2004

- Ahmadinia A., Bobda C., Bednara M., Teich J.:

[A New Approach for On-line Placement on Reconfigurable Devices](#)

International Parallel and Distributed Processing Symposium (IPDPS-2004), Reconfigurable Architectures Workshop (RAW-2004), (Santa Fé NM, 26. April 2004 - 30. April 2004)

In: **Proc. of the International Parallel and Distributed Processing Symposium (IPDPS-2004), Reconfigurable Architectures Workshop 2004**

BibTeX: [Download](#)

- Ahmadinia A., Bobda C., Danne K., Teich J.:

[Generation of Distributed Arithmetic Designs for Reconfigurable Applications](#)

GI/ITG Dynamically Reconfigurable Systems Workshop at the 17th International Conference on Architecture of Computing Systems Organic and Pervasive Computing (Augsburg)

In: **GI/ITG Dynamically Reconfigurable Systems Workshop at the 17th International Conference on Architecture of Computing Systems Organic and Pervasive Computing 2004**

BibTeX: [Download](#)

- Ahmadinia A., Bobda C., Ding J., Teich J.:

[Design and Implementation of Reconfigurable Multiple Bus on Chip \(RMBoC\)](#)

In: **Technical Report 02-2004**, 2004

BibTeX: [Download](#)

(Techreport)

- Ahmadinia A., Bobda C., Fekete SP., Teich J., Van Der Veen JC.:
[**Optimal Routing-Conscious Dynamic Placement for Reconfigurable Devices**](#)
International Conference on Field-Programmable Logic and Applications (FPL)
(Antwerp, 30. August 2004 - 1. September 2004)
In: **Proceedings of International Conference on Field-Programmable Logic and Applications (FPL)**, Berlin: 2004
BibTeX: [Download](#)
- Ahmadinia A., Bobda C., Kalte H., Koch D., Teich J.:
[**FPGA Architecture Extensions for Preemptive Multitasking and Hardware Defragmentation**](#)
IEEE International Conference on Field-Programmable Technology (FPT) (Brisbane, 6. Dezember 2004 - 8. Dezember 2004)
In: **Proceedings of the 2004 IEEE International Conference on Field-Programmable Technology 2004**
BibTeX: [Download](#)
- Ahmadinia A., Bobda C., Koch D., Majer M., Teich J.:
[**A Dynamic NoC Approach for Communication in Reconfigurable Devices**](#)
International Conference on Field-Programmable Logic and Applications (FPL)
(Antwerp, 30. August 2004 - 1. September 2004)
In: **Proceedings of International Conference on Field-Programmable Logic and Applications (FPL)**, London: 2004
BibTeX: [Download](#)
- Ahmadinia A., Bobda C., Koch D., Majer M., Teich J.:
[**Task Scheduling for Heterogeneous Reconfigurable Computers**](#)
17th Symposium on Integrated Circuits and Systems Design (SBCCI) (Pernambuco, 7. September 2004 - 11. September 2004)
In: **Proceedings of the 17th Symposium on Integrated Circuits and Systems Design (SBCCI) 2004**
BibTeX: [Download](#)

- Ahmadinia A., Bobda C., Teich J.:
[A Dynamic Scheduling and Placement Algorithm for Reconfigurable Hardware](#)
17th International Conference on Architecture of Computing Systems (ARCS 2004) (Augsburg, 23. März 2004 - 26. März 2004)
In: **Proceedings of 17th International Conference on Architecture of Computing Systems, Lecture Notes in Computer Science**, Berlin, Heidelberg: 2004
BibTeX: [Download](#)
- Bambha N., Bhattacharyya SS., Teich J., Zitzler E.:
[Systematic Integration of Parameterized Local Search Techniques in Evolutionary Algorithms](#)
Genetic and Evolutionary Computation Conference (Seattle, Washington, 26. Juni 2004 - 30. Juni 2004)
In: **Proceedings of the Genetic and Evolutionary Computation Conference**, Berlin, Heidelberg: 2004
BibTeX: [Download](#)
- Bambha N., Bhattacharyya SS., Zitzler E., Teich J.:
[Systematic Integration of Parameterized Local Search Into Evolutionary Algorithms](#)
In: **IEEE Transactions on Evolutionary Computation** 8 (2004), p. 137-155
ISSN: 1089-778X
DOI: [10.1109/TEVC.2004.823471](#)
BibTeX: [Download](#)
- Bhattacharyya SS., Deprettere E., Teich J.:
[Chapter 6 in Domain-Specific Processors: Systems, Architectures, Modeling, and Simulation](#)
New York, U.S.A.: Marcel Dekker, 2004
(Signal Processing and Communication)
ISBN: 0-8247-4711-9
BibTeX: [Download](#)
- Frauenheim T., Hoffmann M., König P., Mostaghim S., Teich J.:
[Molecular Force Field Parameterization using Multi-Objective Evolutionary Algorithms](#)

Congress on Evolutionary Computation (CEC '04) (Portland, 20. Juni 2004 - 23. Juni 2004)

In: **Proceedings of the Congress on Evolutionary Computation (CEC '04) 2004**

BibTeX: [Download](#)

- Hannig F., Dutta H., Teich J.:

[Mapping of Regular Nested Loop Programs to Coarse-grained Reconfigurable Arrays -- Constraints and Methodology](#)

18th International Parallel and Distributed Processing Symposium (IPDPS 2004), (Santa Fe, NM, 26. April 2004 - 30. April 2004)

In: **Proceedings of the 18th International Parallel and Distributed Processing Symposium 2004**

BibTeX: [Download](#)

- Hannig F., Dutta H., Teich J.:

[Regular Mapping for Coarse-grained Reconfigurable Architectures](#)

IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP) (Montreal, Quebec, 17. Mai 2004 - 21. Mai 2004)

In: **Proceedings of the 2004 IEEE International Conference on Acoustics, Speech, and Signal Processing 2004**

BibTeX: [Download](#)

- Hannig F., Kupriyanov O., Teich J.:

[Automatic and Optimized Generation of Compiled High-Speed RTL Simulators](#)

Workshop on Compilers and Tools for Constrained Embedded Systems (CTCES 2004) (Washington, DC)

In: **Proceedings of the Workshop on Compilers and Tools for Constrained Embedded Systems (CTCES 2004) 2004**

BibTeX: [Download](#)

- Hannig F., Teich J.:

[Dynamic Piecewise Linear/Regular Algorithms](#)

Fourth International Conference on Parallel Computing in Electrical Engineering (PARELEC) (Dresden, 7. September 2004 - 10. September 2004)

In: **Proceedings of the Fourth International Conference on Parallel Computing in Electrical Engineering (PARELEC 2004) 2004**

BibTeX: [Download](#)

- Hannig F., Teich J.:

[Energy Estimation and Optimization for Piecewise Regular Processor Arrays](#)

In: **Chapter 6 in Domain-Specific Processors: Systems, Architectures, Modeling, and Simulation**, New York, U.S.A.,: Marcel Dekker, 2004, p. 107-126 (Signal Processing and Communication)

ISBN: 0-8247-4711-9

BibTeX: [Download](#)

- Hannig F., Teich J.:

[Resource Constrained and Speculative Scheduling of an Algorithm Class with Run-Time Dependent Conditionals](#)

15th IEEE International Conference on Application-specific Systems, Architectures, and Processors (ASAP) (Galveston, TX, 27. September 2004 - 29. September 2004)

In: **Proceedings of the 15th IEEE International Conference on Application-specific Systems, Architectures, and Processors (ASAP 2004) 2004**

BibTeX: [Download](#)

- Hannig F., Teich J.:

[Resource Constrained and Speculative Scheduling of Dynamic Piecewise Regular Algorithms](#)

In: **Technical Report 01-2004**, 2004

BibTeX: [Download](#)

(Techreport)

- Haubelt C., Koch D., Teich J.:

[Basic OS support for distributed reconfigurable hardware](#)

International Workshop on Systems, Architectures, Modeling and Simulation (SAMOS'04) (Samos, 19. Juli 2004 - 21. Juli 2004)

In: **Proceedings of the International Workshop on Systems, Architectures, Modeling and Simulation (SAMOS'04) 2004**

URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=35048878778&origin=inward>

BibTeX: [Download](#)

- Haubelt C., Teich J.:

[Modeling and Analysis of Distributed Reconfigurable Hardware](#)

Dresdener Arbeitstagung Schaltungs- und Systementwurf (DASS 2004) (Dresden, 19. April 2004 - 20. April 2004)

In: **Proc Dresdener Arbeitstagung Schaltungs- und Systementwurf (DASS 2004) 2004**

BibTeX: [Download](#)

- Koch D., Teich J.:

[Platform-Independent Methodology for Partial Reconfiguration](#)

ACM Conference Computing Frontiers (CF 04), (Ischia, 14. April 2004 - 16. April 2004)

In: **Proceedings of the 2004 ACM conference Computing Frontiers 2004**

BibTeX: [Download](#)

- Kupriyanov O., Hannig F., Teich J.:

[High-speed event-driven RTL compiled simulation](#)

International Workshop on Systems, Architectures, Modeling and Simulation (SAMOS'04) (Samos, 19. Juli 2004 - 21. Juli 2004)

In: **Proceedings of the International Workshop on Systems, Architectures, Modeling and Simulation (SAMOS'04) 2004**

URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=35048851603&origin=inward>

BibTeX: [Download](#)

- Mostaghim S., Teich J.:

[Covering Pareto-optimal fronts by subswarms in multi-objective particle swarm optimization](#)

Proceedings of the 2004 Congress on Evolutionary Computation, CEC2004 (Portland, OR, 20. Juni 2004 - 23. Juni 2004)

In: **Proceedings of the Congress on Evolutionary Computation (CEC '04) 2004**

URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=4344649636&origin=inward>

BibTeX: [Download](#)

- Mostaghim S., Teich J.:

[Multi-Objective Particle Swarm Optimization](#)

Dagstuhl Seminar No. 04461

In: **Dagstuhl Seminar No. 04461** 2004

BibTeX: [Download](#)

- Teich J., Bhattacharyya SS.:

[Analysis of Dataflow Programs with Interval-Limited Data-Rates](#)

Computer Systems: Architectures, Modeling, and Simulation (Samos, 19. Juli 2004 - 21. Juli 2004)

In: **Computer Systems: Architectures, Modeling, and Simulation**, Berlin: 2004

BibTeX: [Download](#)

2003

- Ahmadinia A., Bobda C., Danne K., Teich J.:

[A New Approach for Reconfigurable Massively Parallel Computers](#)

IEEE International Conference on Field-Programmable Technology, (Tokyo, 15. Dezember 2003 - 17. Dezember 2003)

In: **Proceedings of the IEEE International Conference on Field-Programmable Technology** 2003

DOI: [10.1109/FPT.2003.1275784](https://doi.org/10.1109/FPT.2003.1275784)

BibTeX: [Download](#)

- Ahmadinia A., Bobda C., Teich J.:

[Temporal Task Clustering for Online Placement on Reconfigurable Hardware](#)

IEEE International Conference on Field-Programmable Technology, (Tokyo, Japan, 15. Dezember 2003 - 17. Dezember 2003)

In: **Proceedings of the IEEE International Conference on Field-Programmable Technology** 2003

BibTeX: [Download](#)

- Ahmadinia A., Teich J.:
[Speeding up Online Placement for XILINX FPGAs by Reducing Configuration Overhead](#)
IFIP International Conference on VLSI-SOC, (Darmstadt, 1. Dezember 2003 - 3. Dezember 2003)
In: **Proceedings of the IFIP International Conference on VLSI-SOC 2003**
BibTeX: [Download](#)
- Bednara M., Danne K., Deppe M., Oberschelp O., Slomka F., Teich J.:
[Design and Implementation of Digital Linear Control Systems on Reconfigurable Hardware](#)
In: **EURASIP J APPL SIG P** (2003), p. 1-9
ISSN: 1110-8657
DOI: [10.1155/S1110865703301040](#)
BibTeX: [Download](#)
- Bednara M., Grabbe C., J. Shokrollahi J., Teich J., von zur Gathen J.:
[A High Performance VLIW Processor for Finite Field Arithmetic](#)
International Parallel and Distributed Processing Symposium (IPDPS-2003), (Nice)
In: **Proceedings of the International Parallel and Distributed Processing Symposium (IPDPS-2003) 2003**
BibTeX: [Download](#)
- Bhattacharyya SS., Deprettere E., Teich J.:
[Domain-Specific Processors: Systems, Architectures, Modeling and Simulation](#)
New York: Marcel Dekker, 2003
(Domain-Specific Processors: Systems, Architectures, Modeling and Simulation)
BibTeX: [Download](#)
- Dellnitz M., Mostaghim S., Schütze O., Teich J.:
[Covering Pareto Sets by Multilevel Evolutionary Subdivision Techniques](#)
Second International Conference on Evolutionary Multi-Criterion Optimization (EMO), (Faro)
In: **Proceedings of the Second International Conference on Evolutionary**

Multi-Criterion Optimization (EMO) 2003

BibTeX: [Download](#)

- Feldmann R., Haubelt C., Monien B., Teich J.:
[Fault tolerance analysis of distributed reconfigurable systems using SAT-based techniques](#)
13th International Conference on Field Programmable Logic and Applications (Lisbon, 1. September 2003 - 3. September 2003)
In: **Proceedings of 13th International Conference on Field Programmable Logic and Applications 2003**
URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=35248814417&origin=inward>
BibTeX: [Download](#)
- Fischer D., Teich J., Thies M., Weper R.:
[Buildabong: A framework for architecture/compiler co-exploration for ASIPs](#)
In: **Journal of Circuits Systems and Computers** 12 (2003), p. 353-375
ISSN: 0218-1266
DOI: [10.1142/S0218126603000799](https://doi.org/10.1142/S0218126603000799)
BibTeX: [Download](#)
- Gerling J., Mrozynski G., Schrage J., Stübbe O., Teich J.:
[Improved time domain simulation of optical multimode intrasystem interconnects](#)
Design, Automation and Test in Europe (DATE 2003), (Munich, 3. März 2003 - 7. März 2003)
In: **Proceedings of Design, Automation and Test in Europe 2003**
DOI: [10.1109/DATE.2003.1253758](https://doi.org/10.1109/DATE.2003.1253758)
BibTeX: [Download](#)
- Grabbe C., Bednara M., Teich J., von zur Gathen J., J. Shokrollahi J.:
[FPGA designs of parallel high performance GF\(2²³³\) multipliers](#)
Proceedings of the 2003 IEEE International Symposium on Circuits and Systems (Bangkok, 25. Mai 2003 - 28. Mai 2003)
In: **Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS-2003) 2003**

URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=0038790049&origin=inward>

BibTeX: [Download](#)

- Haubelt C., Koch D., Teich J.:

[Basic OS Support for Distributed Reconfigurable Hardware](#)

Third International Workshop on Systems, Architectures, Modeling and Simulation (SAMOS'03) (Samos, 21. Juli 2003 - 23. Juli 2003)

In: **Proceedings of the Third International Workshop on Systems, Architectures, Modeling and Simulation (SAMOS'03) 2003**

BibTeX: [Download](#)

- Haubelt C., Koch D., Teich J.:

[ReCoNet: Modeling and implementation of fault tolerant distributed reconfigurable hardware](#)

16th Symposium on Integrated Circuits and Systems Design, SBCCI 2003 (São Paulo, 8. September 2003 - 11. September 2003)

In: **Proceedings of the 16th Symposium on Integrated Circuits and Systems Design (SBCCI2003) 2003**

DOI: [10.1109/SBCCI.2003.1232851](https://doi.org/10.1109/SBCCI.2003.1232851)

BibTeX: [Download](#)

- Haubelt C., Mostaghim S., Slomka F., Teich J., Tyagi A.:

[Hierarchical Synthesis of Embedded Systems Using Evolutionary Algorithms](#)

In: Drechsler, R. and Drechsler, N (ed.): **Evolutionary Algorithms in System Design**, Boston, Dordrecht, London: Kluwer Academic Publishers, 2003, p. 63-104 (Genetic Algorithms and Evolutionary Computation (GENA))

BibTeX: [Download](#)

- Haubelt C., Teich J.:

[Accelerating Design Space Exploration](#)

5th International Conference on ASIC (ASICON 2003) (Beijing, 21. Oktober 2003 - 24. Oktober 2003)

In: **Proceedings of 5th International Conference on ASIC (ASICON 2003) 2003**

BibTeX: [Download](#)

- Haubelt C., Teich J.:
[Accelerating design space exploration using Pareto-front arithmetics \[SoC design\]](#)
Asia and South Pacific Design Automation Conference, ASP-DAC 2003
(Kitakyushu, 21. Januar 2003 - 24. Januar 2003)
In: **Proceedings ASP-DAC 2003, Asia and South Pacific Design Automation Conference 2003**
DOI: [10.1109/ASPDAC.2003.1195073](https://doi.org/10.1109/ASPDAC.2003.1195073)
BibTeX: [Download](#)
- Haubelt C., Teich J., Feldmann R., Monien B.:
[SAT-based techniques in system synthesis](#)
Design, Automation and Test in Europe Conference and Exhibition, DATE 2003
(Munich, 3. März 2003 - 7. März 2003)
In: **Proceedings of Design, Automation and Test in Europe (DATE 2003) 2003**
DOI: [10.1109/DATE.2003.1253784](https://doi.org/10.1109/DATE.2003.1253784)
BibTeX: [Download](#)
- Kralicek P., John W., Reinhold C., Teich J.:
[Synthesizing Passive Networks by applying Genetic Programming and Evolution Strategies](#)
Congress on Evolutionary Computation (CEC'03), (Canberra, 8. Dezember 2003 - 12. Dezember 2003)
In: **Proceedings of the Congress on Evolutionary Computation (CEC'03) 2003**
DOI: [10.1109/CEC.2003.1299883](https://doi.org/10.1109/CEC.2003.1299883)
BibTeX: [Download](#)
- Mostaghim S., Teich J.:
[Strategies for finding good local guides in multi-objective particle swarm optimization](#)
Swarm Intelligence Symposium (Indianapolis, 24. April 2003 - 26. April 2003)
In: **Proceedings of the Swarm Intelligence Symposium 2003**
BibTeX: [Download](#)

- Mostaghim S., Teich J.:
[The role of e-dominance in Multi-Objective Particle Swarm Optimization Methods](#)
2003 Congress on Evolutionary Computation, CEC 2003 (Canberra, 8. Dezember 2003 - 12. Dezember 2003)
In: **Proceedings of the Congress on Evolutionary Computation (CEC'03) 2003**
DOI: [10.1109/CEC.2003.1299886](https://doi.org/10.1109/CEC.2003.1299886)
BibTeX: [Download](#)
- Teich J.:
[Entwurfsautomatisierung elektronischer Systeme auf Systemebene](#)
11. EIS-Workshop, Entwurf Integrierter Schaltungen und Systeme, (Erlangen)
In: **VDE/VDI-Gesellschaft Mikroelektronik, Mikro- und Feinwerktechnik (GMM), GMM-Fachbericht**, Berlin: 2003
BibTeX: [Download](#)
- Teich J., Bednara M.:
[Automatic Synthesis of FPGA Processor Arrays from Loop Algorithms](#)
In: **Journal of Supercomputing** (2003), p. 149-165
ISSN: 0920-8542
DOI: [10.1023/A:1024447517501](https://doi.org/10.1023/A:1024447517501)
BibTeX: [Download](#)
- Teich J., Haubelt C., Mostaghim S., Tyagi A.:
[Solving hierarchical optimization problems using MOEAs](#)
In: Carlos M. Fonseca, Peter J. Fleming, Eckart Zitzler, Kalyanmoy Deb, and Lothar Thiele (ed.): **Evolutionary Multi-Criterion Optimization**, Berlin, Heidelberg, New York: Springer, 2003, p. 162-176 (Lecture Notes in Computer Science, Vol.2632)
URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=35248891516&origin=inward>
BibTeX: [Download](#)
- Teich J., Slomka F.:
[A Model for Buffer Exploration in EDF Scheduled Embedded Systems](#)
11. EIS-Workshop, Entwurf Integrierter Schaltungen und Systeme, (Erlangen)

In: **VDE/VDI-Gesellschaft Mikroelektronik, Mikro- und Feinwerktechnik (GMM), GMM-Fachbericht**, Berlin: 2003

BibTeX: [Download](#)

2002

- Bednara M., Daldrup M., J. Shokrollahi J., Teich J., von zur Gathen J.:
[Tradeoff Analysis of FPGA Based Elliptic Curve Cryptography](#)
IEEE International Symposium on Circuits and Systems (ISCAS-02), (Scottsdale, Arizona, 26. Mai 2002 - 29. Mai 2002)
In: **Proc. of IEEE International Symposium on Circuits and Systems 2002**
BibTeX: [Download](#)
- Bednara M., J. Shokrollahi J., Teich J., Daldrup M., von zur Gathen J.:
[Reconfigurable Implementation of Elliptic Curve Crypto Algorithms](#)
9th Reconfigurable Architectures Workshop, (Fort Lauderdale, Florida)
In: **Proc. The 9th Reconfigurable Architectures Workshop 2002**
BibTeX: [Download](#)
- Bednara M., Teich J.:
[Interface Synthesis for FPGA Based VLSI Processor Arrays](#)
The International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA02), (Las Vegas, Nevada, 24. Juni 2002 - 27. Juni 2002)
In: **Proc. of The International Conference on Engineering of Reconfigurable Systems and Algorithms 2002**
BibTeX: [Download](#)
- Deprettere E., Teich J., Vassiliadis S.:
[Embedded Processor Design Challenges](#)
In: **Embedded Processor Design Challenges**, Berlin, Germany: Springer, 2002
(Lecture Notes in Computer Science (LNCS), Vol. Vol. 2268)
BibTeX: [Download](#)
- Fischer D., Teich J., Thies M., Weper R.:
[Architecture/Compiler Co-Exploration for ASIPs](#)
In: **International Journal of Circuits, Systems and Signal Processing (2002)**
ISSN: 1998-4464
BibTeX: [Download](#)

- Fischer D., Teich J., Thies M., Weper R.:
[Efficient Architecture/Compiler Co-Exploration for ASIPs](#)
International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES2002), (Grenoble, 8. Oktober 2002 - 11. Oktober 2002)
In: **ACM SIG Proceedings of the International Conference on Compilers, Architecture, and Synthesis for Embedded Systems 2002**
DOI: [10.1145/581630.581635](https://doi.org/10.1145/581630.581635)
BibTeX: [Download](#)
- Hannig F., Teich J.:
[Energy Estimation for Piecewise Regular Processor Arrays](#)
Second International Samos Workshop on Systems, Architectures, Modeling, and Simulation (SAMOS 2002), (Island of Samos, 22. Juli 2002 - 25. Juli 2002)
In: **Proceedings of the Second International Samos Workshop on Systems, Architectures, Modeling, and Simulation 2002**
BibTeX: [Download](#)
- Hannig F., Teich J.:
[Energy Estimation of Nested Loop Programs](#)
14th Annual ACM Symposium on Parallel Algorithms and Architectures (SPAA 2002), (Winnipeg, Manitoba, 10. August 2002 - 13. August 2002)
In: **Proceedings 14th Annual ACM Symposium on Parallel Algorithms and Architectures 2002**
BibTeX: [Download](#)
- Hannig F., Teich J., Bednara M.:
[Generation of Distributed Loop Control](#)
In: E. Deprettere, J. Teich, and S. Vassiliadis (ed.): **Embedded Processor Design Challenges, Lecture Notes in Computer Science (LNCS)**, Berlin, Germany: Springer, 2002, p. 154-170
BibTeX: [Download](#)
- Haubelt C., Teich J., Richter K., Ernst R.:
[Flexibility/cost-tradeoffs of platform-based systems](#)
In: E. Deprettere, J. Teich, and S. Vassiliadis (ed.): **Embedded Processor Design Challenges**, Springer Verlag, 2002, p. 38-56 (Lecture Notes in Computer Science (LNCS), Vol.2268)

ISBN: 9783540433224

URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=84893789262&origin=inward>

BibTeX: [Download](#)

- Haubelt C., Teich J., Richter K., Ernst R.:

[Modellierung Rekonfigurierbarer Systemarchitekturen](#)

GI / ITG / GMM Workshop - Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (Tuebingen)

BibTeX: [Download](#)

- Haubelt C., Teich J., Richter K., Ernst R.:

[System design for flexibility](#)

2002 Design, Automation and Test in Europe Conference and Exhibition, DATE 2002 (Paris)

In: **Proc. DATE 2002, Design, Automation and Test in Europe 2002**

DOI: [10.1109/DATE.2002.998399](https://doi.org/10.1109/DATE.2002.998399)

BibTeX: [Download](#)

- Mostaghim S., Teich J., Tyagi A.:

[Comparison of data structures for storing Pareto-sets in MOEAs](#)

2002 Congress on Evolutionary Computation, CEC 2002 (Honolulu, HI)

DOI: [10.1109/CEC.2002.1007035](https://doi.org/10.1109/CEC.2002.1007035)

BibTeX: [Download](#)

- Köster M., Teich J.:

[\(Self-\)reconfigurable finite state machines: Theory and implementation](#)

2002 Design, Automation and Test in Europe Conference and Exhibition, DATE 2002 (Paris)

In: **Proc. DATE 2002, Design, Automation and Test in Europe 2002**

DOI: [10.1109/DATE.2002.998356](https://doi.org/10.1109/DATE.2002.998356)

BibTeX: [Download](#)

- Teich J., Ernst R., Richter K., Thiele L., Ziegenbein D.:

[SPI - A System Model for Heterogeneously Specified Embedded Systems](#)

In: **IEEE Transactions on Very Large Scale Integration (VLSI) Systems** 10 (2002), p. 379-389

ISSN: 1063-8210

DOI: [10.1109/TVLSI.2002.807767](https://doi.org/10.1109/TVLSI.2002.807767)

BibTeX: [Download](#)

- Teich J., Thiele L.:

[Exact Partitioning of Affine Dependence Algorithms](#)

In: **Embedded Processor Design Challenges, Lecture Notes in Computer Science (LNCS)**, Berlin, Germany: Springer, 2002, p. 135-151

BibTeX: [Download](#)

2001

- Anlauff M., Fischer D., Kutter P., Teich J., Weper R.:

[Hierarchical Microprocessor Design Using XASM](#)

EUROCAST 2001 (Las Palmas de Gran Canaria, 19. Februar 2001 - 23. Februar 2001)

In: **Proc. EUROCAST 2001** 2001

BibTeX: [Download](#)

- Bednara M., Beyer O., Teich J., [Wanka R.](#):

[Hardware Supported Sorting: Design and Tradeoff Analysis](#)

In: **In System Design Automation**, Kluwer Academic Publishers, 2001, p. 97-107

BibTeX: [Download](#)

- Bednara M., Hannig F., Teich J.:

[Boundary control: A new distributed control architecture for space-time transformed \(VLSI\) processor arrays](#)

35th Asilomar Conference on Signals, Systems and Computers (Pacific Grove, CA)

In: Matthews M.B. (ed.): **Proc. 35th IEEE Asilomar Conf. on Signals, Systems and Computers** 2001

URL: <https://www.scopus.com/inward/record.url?partnerID=HzOxMe3b&scp=0035573058&origin=inward>

BibTeX: [Download](#)

- Bhattacharyya SS., Teich J., Zitzler E., Bambha N.:

[Hybrid Global/Local Search Strategies for Dynamic Voltage Scaling in Embedded Multiprocessors](#)

9th Int. Workshop on Hardware/Software Co-Design, (Copenhagen, 25. April 2001 - 27. April 2001)

In: **Proc. 9th Int. Workshop on Hardware/Software Co-Design 2001**

BibTeX: [Download](#)

- Cieslok F., Esau H., Teich J.:

[EXPLORA- generic design space exploration during embedded system synthesis](#)

Springer New York LLC, 2001

ISBN: 9781475745351

DOI: [10.1007/978-0-387-35409-5_21](https://doi.org/10.1007/978-0-387-35409-5_21)

BibTeX: [Download](#)

- Ernst R., Griess M., Strehl K., Teich J., Thiele L., Ziegenbein D.:

[FunState - An Internal Design Representation for Codesign](#)

In: **IEEE Transactions on Very Large Scale Integration (VLSI) Systems** (2001),
p. 524-544

ISSN: 1063-8210

DOI: [10.1109/92.931229](https://doi.org/10.1109/92.931229)

BibTeX: [Download](#)

- Fekete SP., Köhler E., Teich J.:

[Extending Partial Suborders](#)

In: Hajo Broersma, Ulrich Faigle, Johann Hurink and Stefan Pickl (ed.): **Electronic Notes in Discrete Mathematics**, Elsevier BV, 2001

BibTeX: [Download](#)

- Fekete SP., Köhler E., Teich J.:

[Higher-Dimensional Packing with Order Constraints](#)

7th Workshop on Algorithms and Data Structures,

In: **Proc. 7th Workshop on Algorithms and Data Structures, Lecture Notes in Computer Science (LNCS), Vol. 2125** 2001

BibTeX: [Download](#)

- Fekete SP., Köhler E., Teich J.:

[Optimal FPGA Module Placement with Temporal Precedence Constraints](#)

DATE 2001, Design, Automation and Test in Europe, (Munich, 13. März 2001 - 16. März 2001)

In: **Proc. DATE 2001, Design, Automation and Test in Europe 2001**

DOI: [10.1109/DATE.2001.915093](https://doi.org/10.1109/DATE.2001.915093)

BibTeX: [Download](#)

- Fekete SP., Schepers J., Teich J.:

[**Optimization of Dynamic Hardware Reconfigurations**](#)

In: **Journal of Supercomputing** (2001), p. 57-75

ISSN: 0920-8542

DOI: [10.1023/A:1011188411132](https://doi.org/10.1023/A:1011188411132)

BibTeX: [Download](#)

- Fischer D., Kastens U., Teich J., Thies M., Weper R.:

[**Design Space Characterization for Architecture/Compiler Co-Exploration**](#)

International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES 2001), (Atlanta, Georgia)

In: **ACM SIG Proceedings International Conference on Compilers, Architectures and Synthesis for Embedded Systems 2001**

BibTeX: [Download](#)

- Fischer D., Teich J., Weper R.:

[**Hierarchical Modeling and Simulation of Embedded Processors Using ASMs**](#)

International Workshop on Software and Compilers for Embedded Systems, (SCOPES 2001), (St. Goar, 20. März 2001 - 22. März 2001)

In: **International Workshop on Software and Compilers for Embedded Systems 2001**

BibTeX: [Download](#)

- Hannig F., Teich J.:

[**Design Space Exploration for Massively Parallel Processor Arrays**](#)

Sixth International Conference on Parallel Computing Technologies (PaCT-2001) (Novosibirsk, 3. September 2001 - 7. September 2001)

In: **Proc. of the Sixth International Conference on Parallel Computing Technologies (PaCT-2001) 2001**

BibTeX: [Download](#)

- Teich J.:

[**Exact Partitioning of Affine Dependence Algorithms**](#)

SAMOS - Systems, Architectures, Modeling and Simulation Workshop, (Island of Samos)

In: **Proc. SAMOS - Systems, Architectures, Modeling and Simulation Workshop 2001**

BibTeX: [Download](#)

- Teich J.:

[Pareto-Front Exploration with Uncertain Objectives](#)

First International Conference on Evolutionary Multi-Criterion Optimization, (Zurich, 7. März 2001 - 9. März 2001)

In: **Proc. First International Conference on Evolutionary Multi-Criterion Optimization, In Lecture Notes in Computer Science (LNCS), Vol. 1993 2001**

BibTeX: [Download](#)

- Teich J.:

[Symbiose von Hardware und Software](#)

In: K. J. Buchenrieder (ed.): **Hardware/Software Codesign**, Bruchsal: IT Press, 2001, p. 79-107 (Informationsverarbeitung und Technische Informatik)

BibTeX: [Download](#)

- Teich J.:

[Synthesis and Optimization of Digital Hardware/Software Systems](#)

In: R. Merker and W. Schwarz (ed.): **In System Design Automation**, Kluwer Academic Publishers, 2001, p. 3-26

BibTeX: [Download](#)

- Teich J., Bednara M.:

[Synthesis of FPGA Implementations from Loop Algorithms](#)

First International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA01), (Las Vegas, Nevada, 25. Juni 2001 - 28. Juni 2001)

In: **Proc. of the First International Conference on Engineering of Reconfigurable Systems and Algorithms 2001**

BibTeX: [Download](#)

2000

- Bednara M., Beyer O., Teich J., [Wanka R.](#):

[Hardware-Supported Sorting: Design and Tradeoff Analysis](#)

Workshop on System Design Automation - SDA 2000 (Rathen)

In: **Workshop on System Design Automation - SDA 2000** 2000

BibTeX: [Download](#)

- Bednara M., Beyer O., Teich J., [Wanka R.](#):

[Tradeoff Analysis and Architecture Design of a Hybrid Hardware/Software Sorter](#)

Int. Conf. on Application Specific Systems, Architectures, and Processors, pp. 299-308, Boston, MA, U.S.A. IEEE Computer Society Press, July 2000 Proc. ASAP'00, the Int. Conf. on Application Specific Systems, Architectures, and Processors, (Boston, MA, 10. Juli 2000 - 12. Juli 2000)

In: **Proc. ASAP'00, the Int. Conf. on Application Specific Systems, Architectures, and Processors, pp. 299-308, Boston, MA, U.S.A. IEEE Computer Society Press, July 2000 Proc. ASAP'00, the Int. Conf. on Application Specific Systems, Architectures, and Processors 2000**

BibTeX: [Download](#)

- Bednara M., Hardt W., Rettberg A., Teich J.:

[Automated Design Space Exploration on System Level for Embedded Systems](#)

Ninth Annual International HDL Conference and Exhibition (HDL Conf. 2000), (San Jose, CA)

In: **Proc. Ninth Annual International HDL Conference and Exhibition 2000**

BibTeX: [Download](#)

- Bhattacharyya SS., Teich J., Zitzler E.:

[Evolutionary Algorithms for the Synthesis of Embedded Software](#)

In: **IEEE Transactions on Very Large Scale Integration (VLSI) Systems** 8 (2000), p. 452-456

ISSN: 1063-8210

DOI: [10.1109/92.863627](https://doi.org/10.1109/92.863627)

BibTeX: [Download](#)

- Bhattacharyya SS., Teich J., Zitzler E.:

[Multidimensional Exploration of Software Implementations for DSP Algorithms](#)

In: **Journal of VLSI Signal Processing** (2000), p. 83-98

ISSN: 0922-5773

DOI: [10.1023/A:1008170728742](https://doi.org/10.1023/A:1008170728742)

BibTeX: [Download](#)

- Bhattacharyya SS., Teich J., Zitzler E.:
[Optimizing the Efficiency of Parameterized Local Search within Global Search](#)
Int. Conf. on Evolutionary Computation, (La Jolla, CA)
In: **Proc. of CEC'2000, the Int. Conf. on Evolutionary Computation 2000**
BibTeX: [Download](#)
- Böke C., Ditze C., Hardt W., Kleinjohann B., Rammig F., Rettberg A., Stroop J., Teich J.:
[P-based System Design with the PARADISE Design Environment](#)
In: **EUROMICRO Journal** (2000)
ISSN: 0167-3858
BibTeX: [Download](#)
- Cieslok F., Ernst R., Jersak M., Richter K., Strehl K., Teich J., Thiele L., Wolf F., Ziegenbein D.:
[Embedded System Design using the SPI Workbench](#)
Forum on Design Languages 2000, (Tübingen)
In: **Proc. FDL'00 2000**
BibTeX: [Download](#)
- Cieslok F., Esau H., Teich J.:
[EXPLORA - Generic Design Space Exploration During Embedded System Synthesis](#)
Int. IFIP Workshop on Distributed and Parallel Embedded Systems, (Schloss Eringerfeld)
In: **Proc. DIPES 2000, Int. IFIP Workshop on Distributed and Parallel Embedded Systems 2000**
BibTeX: [Download](#)
- Ernst R., Richter K., Teich J., Ziegenbein D.:
[SPI Workbench - Entwurf gemischt reaktiv/transformativer Systeme](#)
Workshop Architekturentwurf für eingebettete Systeme, (Karlsruhe)

In: **AES 2000, Workshop Architektorentwurf für eingebettete Systeme 2000**

BibTeX: [Download](#)

- Fischer D., Teich J., Trinkert S., Weper R.:

[A Joined Architecture/Compiler Environment for ASIPs](#)

International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES 2000), (San Jose, CA, 17. November 2000 - 18. November 2000)

In: **ACM SIG Proc. International Conference on Compilers, Architectures and Synthesis for Embedded Systems 2000**

BibTeX: [Download](#)

- Fischer D., Teich J., Trinkert S., Weper R.:

[BUILDABONG: A Rapid Prototyping Environment for ASIPs](#)

DSP-Deutschland 2000, (Munich)

In: **Proc. DSP-Deutschland 2000 2000**

BibTeX: [Download](#)

- Wolfram Hardt, Franz Rammig, Carsten Böke, Joachim Stroop, Achim Rettberg, Del Castillo, Bernd Kleinjohann, Jürgen Teich:

[IP-based System Design within the PARADISE Design Environment](#)

In: **Journal of Systems Architecture (2000)**

ISSN: 1383-7621

BibTeX: [Download](#)

- Kutter P., Teich J., Weper R.:

[Description and Simulation of Microprocessor Instruction Sets Using ASMs](#)

International Workshop on Abstract State Machines (, 19. März 2000 - 24. März 2000)

In: **Lecture Notes in Computer Science (LNCS) 1912 2000**

DOI: [10.1007/3-540-44518-8_15](#)

BibTeX: [Download](#)

- Strehl K., Teich J., Thiele L.:

[Regular State Machines](#)

In: **Parallel Algorithms and Applications (2000), p. 265-300**

ISSN: 1063-7192

BibTeX: [Download](#)

- Teich J.:
[Symbiose von Hardware und Software](#)
In: **ForschungsForum 2000**, 2000, p. 82-87
BibTeX: [Download](#)
(Techreport)

1999

- Bhattacharyya SS., Teich J., Zitzler E.:
[3D Exploration of Software Schedules for DSP Algorithms](#)
7th Int. Workshop on Hardware/Software Co-Design, (Rome, 3. Mai 1999 - 5. Mai 1999)
In: **Proc. CODES'99, the 7th Int. Workshop on Hardware/Software Co-Design 1999**
BibTeX: [Download](#)
- Bhattacharyya SS., Teich J., Zitzler E.:
[Evolutionary Algorithm Based Exploration of Software Schedules for Digital Signal Processors](#)
Genetic and Evolutionary Computation Conference, (Orlando, Florida)
In: **Proc. GECCO'99, the Genetic and Evolutionary Computation Conference 1999**
BibTeX: [Download](#)
- Bhattacharyya SS., Teich J., Zitzler E.:
[Optimized Software Synthesis for DSP Using Randomization Techniques](#)
In: **Technical Report No. 75**, 1999
BibTeX: [Download](#)
(Techreport)
- Ernst R., Richter K., Teich J., Thiele L., Ziegenbein D.:
[Hardware/Software Codesign of Embedded Systems - The SPI Workbench](#)
Int. Workshop on VLSI, (Orlando, Florida)
In: **Proc. Int. Workshop on VLSI 1999**
BibTeX: [Download](#)
- Ernst R., Richter K., Teich J., Thiele L., Ziegenbein D.:
[Representation of Function Variants for Embedded System Optimization](#)

and Synthesis

36th Design Automation Conference (DAC), (New Orleans, 21. Juni 1999 - 25. Juni 1999)

In: **Proc. 36th Design Automation Conference 1999**

BibTeX: [Download](#)

- Ernst R., Richter K., Teich J., Thiele L., Ziegenbein D.:

[SPI - An Internal Representation for Heterogeneously Specified Embedded Systems](#)

GI/ITG/GMM Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, (Braunschweig)

In: **Proc. GI/ITG/GMM Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen 1999**

BibTeX: [Download](#)

- Ernst R., Strehl K., Teich J., Thiele L., Ziegenbein D.:

[FunState - An Internal Design Representation for Codesign](#)

IEEE/ACM Int. Conf. on Computer-Aided Design, (San Jose, CA, 7. November 1999 - 11. November 1999)

In: **Proc. ICCAD'99, the IEEE/ACM Int. Conf. on Computer-Aided Design 1999**

BibTeX: [Download](#)

- Ernst R., Strehl K., Teich J., Thiele L., Ziegenbein D.:

[Scheduling Hardware/Software Systems Using Symbolic Techniques](#)

7th Int. Workshop on Hardware/Software Co-Design, (Rome, 3. Mai 1999 - 5. Mai 1999)

In: **Proc. CODES'99, the 7th Int. Workshop on Hardware/Software Co-Design 1999**

BibTeX: [Download](#)

- Fekete SP., Schepers J., Teich J.:

[Compile-Time Optimization of Dynamic Hardware Reconfigurations](#)

Int. Conf. on Parallel and Distributed Processing Techniques and Applications (PDPTA'99), (Las Vegas, Nevada)

In: **Proc. Int. Conf. on Parallel and Distributed Processing Techniques and Applications 1999**

BibTeX: [Download](#)

1998

- Bhattacharyya S., Teich J., Zitzler E.:
[Buffer Memory Optimization in DSP Applications - An Evolutionary Approach](#)
Parallel Problem Solving from Nature (PPSN'98) (Amsterdam)
In: **Springer Lecture Notes in Computer Science (LNCS) 1498** 1998
BibTeX: [Download](#)
- Bhattacharyya S., Teich J., Zitzler E.:
[Optimized Software Synthesis for Digital Processing Algorithms - An Evolutionary Approach](#)
In: **Technical Report No. 32, Computer Engineering and Communication Networks Lab (TIK)**, 1998
BibTeX: [Download](#)
(anderer)
- Bhattacharyya S., Teich J., Zitzler E.:
[Optimized Software Synthesis for Digital Signal Processing Algorithms: An Evolutionary Approach](#)
Workshop on Signal Processing Systems (SiPS), (Boston, 8. Oktober 1998 - 10. Oktober 1998)
In: **Proc. of the 1998 Workshop on Signal Processing Systems** 1998
BibTeX: [Download](#)
- Bhattacharyya SS., Teich J., Zitzler E.:
[Buffer Memory Optimization in DSP Applications - An Evolutionary Approach](#)
In: **Parallel Problem Solving from Nature (PPSN'98)**, Amsterdam, The Netherlands: Springer-verlag, 1998, p. 292-301
ISBN: 3540650784
BibTeX: [Download](#)
- Blickle T., Teich J., Thiele L.:
[System-Level Synthesis Using Evolutionary Algorithms](#)
In: **Design Automation For Embedded Systems** 3 (1998), p. 23-58
ISSN: 0929-5585
BibTeX: [Download](#)

- Eisenring M., Teich J.:
[Domain-Specific Interface Generation From Dataflow Specifications](#)
6th Int. Workshop on Hardware/Software Co-design, (Seattle, Washington, 15. März 1998 - 18. März 1998)
In: **Proc. of Codes/CASHE'98, the 6th Int. Workshop on Hardware/Software Co-design 1998**
BibTeX: [Download](#)
- Eisenring M., Teich J.:
[Interfacing Hardware and Software](#)
Proc. of FPL'98, the Conf. on Field-Programmable Logic and Applications (Tallin)
In: **Proc. of FPL'98, the Conf. on Field-Programmable Logic and Applications, Tallin, Estonia, Springer Lecture Notes in Computer Science (LNCS) 1482 1998**
BibTeX: [Download](#)
- Eisenring M., Teich J., Thiele L.:
[Rapid Prototyping of Dataflow Programs on Hardware/Software Architectures](#)
Hawai'i Int. Conf. on Syst. Sci., (Kona, Hawaii, 6. Januar 1998 - 9. Januar 1998)
In: **Proc. of HICSS'98, the Hawai'i Int. Conf. on Syst. Sci. 1998**
BibTeX: [Download](#)
- Ernst R., Richter K., Teich J., Thiele L., Ziegenbein D.:
[Combining Multiple Models of Computation for Scheduling and Allocation](#)
Codes/CASHE'98, the 6th Int. Workshop on Hardware/Software Codesign (Seattle, Washington)
In: **Proc. of Codes/CASHE'98, the 6th Int. Workshop on Hardware/Software Codesign 1998**
BibTeX: [Download](#)
- Ernst R., Richter K., Teich J., Thiele L., Ziegenbein D.:
[Representation of Process Mode Correlation for Scheduling](#)
ICCAD - the ACM/IEEE Int. Conf. on CAD (San Jose, CA, 8. November 1998 - 12. November 1998)
In: **Proc. of ICCAD - the ACM/IEEE Int. Conf. on CAD 1998**
BibTeX: [Download](#)

- Esser R., Teich J., Thiele L.:
[CodeSign: An Embedded System Design Environment](#)
In: **IEE Proceedings E: Computers and Digital Techniques** 145 (1998), p. 171-180
ISSN: 0143-7062
BibTeX: [Download](#)
- Naedele M., Strehl K., Teich J., Thiele L., Ziegenbein D.:
[SCF - State Machine Controlled Flow Diagrams](#)
In: Swiss Federal Institute of Technology (ETH) Zurich (ed.): **Technical Report No. 32, Computer Engineering and Communication Networks Lab (TIK)**, 1998
BibTeX: [Download](#)
(anderer)
- Teich J., Fekete S., Schepers J.:
[Optimizing Dynamic Hardware Reconfigurations](#)
(1998)
BibTeX: [Download](#)
(anderer)
- Teich J., Thiele L.:
[Regular State Machines](#)
Workshop Seminar No. 98341, Tiling for Optimal Resource Utilization, Schloss Dagstuhl (Schloss Dagstuhl)
In: **Presented at Workshop Seminar No. 98341, Tiling for Optimal Resource Utilization** 1998
BibTeX: [Download](#)
- Teich J., Zitzler E.:
[3D Exploration of Uniprocessor Schedules for DSP Algorithms](#)
(1998)
BibTeX: [Download](#)
(anderer)

1997

- Blickle T., Teich J., Thiele L.:
[An Evolutionary Approach to System-Level Synthesis](#)
Codes/CASHE'97, the 5th Int. Workshop on Hardware/Software Co-design (Braunschweig)
In: **Proc. of Codes/CASHE'97, the 5th Int. Workshop on Hardware/Software Co-design, Braunschweig, Germany, pp. 167-171, March 1997** 1997
BibTeX: [Download](#)
- Fortes J., Noll T., Taylor V., Teich J., Thiele L., Vissers K.:
[Proc. IEEE Int. Conference on Application Specific Systems, Architectures, and Processors \(ASAP'97\)](#)
IEEE Computer Society Press, 1997
BibTeX: [Download](#)
- Martin M., Sriram S., Teich J., Thiele L.:
[Performance Analysis of Mixed Asynchronous-Synchronous Systems](#)
In: **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems** 16 (1997), p. 473-484
ISSN: 0278-0070
BibTeX: [Download](#)
- Teich J.:
[Digitale Hardware/Software-Systeme: Synthese und Optimierung](#)
Springer, 1997
BibTeX: [Download](#)
- Teich J.:
[Hardware/Software-Codesign: Massgeschneiderte elektronische Systeme. Teil II: HW/SW-Synthese](#)
In: **Bulletin SEV/VSE** (1997), p. 17-22
BibTeX: [Download](#)
- Teich J., Thiele L., Zhang L.:
[Partitioning Processor Arrays under Resource Constraints](#)
In: **Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology** 17 (1997), p. 5-20

ISSN: 1387-5485

BibTeX: [Download](#)

1996

- Teich J.:
[Hardware/Software-Codesign: Massgeschneiderte elektronische Systeme. Teil I: HW/SW-Architekturen und Spezifikation](#)
In: **Bulletin SEV/VSE** (1996), p. 17-23
BibTeX: [Download](#)
- Teich J.:
[Synthesis and Optimization of Digital Hardware/Software Systems](#) (Habilitationsschrift, 1996)
BibTeX: [Download](#)
- Teich J., Blickle T., Thiele L.:
[An evolutionary approach to system-level synthesis](#)
1st Online Workshop on Soft Computing (Nagoya, Japan)
In: **Proc. of WSC1, the 1st Online Workshop on Soft Computing 1996**
BibTeX: [Download](#)
- Teich J., Thiele L.:
[A new approach to solving resource-constrained scheduling problems based on a flow-model](#)
In: Swiss Federal Institute of Technology (ETH) Zurich (ed.): **Technical Report No. 17, Computer Engineering and Communication Networks Lab (TIK)**, 1996
BibTeX: [Download](#)
(anderer)
- Teich J., Thiele L.:
[System-level synthesis using evolutionary algorithms](#)
(1996)
BibTeX: [Download](#)
(anderer)
- Teich J., Thiele L., Zhang L.:
[Scheduling of partitioned regular algorithms on processor arrays with](#)

constrained resources

Int. Conf. on Application-Specific Systems, Architectures, and Processors (ASAP'96), (Chicago, U.S.A., 19. August 1996 - 21. August 1996)

In: **Proc. Int. Conf. on Application-Specific Systems, Architectures, and Processors (ASAP'96)Int. Conf. on Application-Specific Systems, Architectures, and Processors (ASAP'96)Int. Conf. on Application-Specific Systems, Architectures, and Processors 1996**

BibTeX: [Download](#)

1995

- Evans BL., Schwarz C., Teich J., Welzl E.:

On finding a minimal enclosing parallelogram

11th ACM Symposium on Computational Geometry (Vancouver, British Columbia)

In: **In Proc. 11th ACM Symposium on Computational Geometry 1995**

BibTeX: [Download](#)

- Teich J., Lee EA., Thiele L.:

Modeling and simulation of heterogeneous real-time systems based on a deterministic discrete event model

8th Int. Symposium on System Level Synthesis (ISSS'95), (Cannes, France,)

In: **Proc. of the 8th Int. Symposium on System Level Synthesis 1995**

DOI: [10.1109/ISSS.1995.520628](https://doi.org/10.1109/ISSS.1995.520628)

BibTeX: [Download](#)

1994

- Evans BL., Kalker TA., Teich J.:

Families of Smith Form Decompositions to simplify Multidimensional Filter Design

IEEE Asilomar Conf. on Signals, Systems and Computers, (Pacific Grove, CA, U.S.A.,)

In: **Proc. IEEE Asilomar Conf. on Signals, Systems and Computers 1994**

BibTeX: [Download](#)

- Evans BL., Schwarz C., Teich J.:
[Automated design of two-dimensional rational decimation systems](#)
IEEE Asilomar Conf. on Signals, Systems and Computers, (Pacific Grove, CA, U.S.A.,)
In: **Proc. IEEE Asilomar Conf. on Signals, Systems and Computers 1994**
BibTeX: [Download](#)
- Evans BL., Schwarz C., Teich J., Welzl E.:
[On finding a minimal enclosing parallelogram](#)
4th MSI Workshop on Computational Geometry, (Cornell University, Ithaca, NY, U.S.A.,)
In: ICSI - International Computer Science Institute, Berkeley (ed.): **4th MSI Workshop on Computational Geometry 1994**
BibTeX: [Download](#)
- Martin M., Sriram S., Teich J., Thiele L.:
[Performance analysis and optimization of mixed asynchronous synchronous systems](#)
(1994)
BibTeX: [Download](#)
(anderer)
- Martin M., Sriram S., Teich J., Thiele L.:
[Performance Analysis of Mixed Asynchronous-Synchronous Systems](#)
EEE Int. Workshop on VLSI Signal Processing 94 (, 26. Oktober 1994 - 28. Oktober 1994)
In: **Proc. of the IEEE Int. Workshop on VLSI Signal Processing 94 1994**
BibTeX: [Download](#)

1993

- Teich J.:
[A Compiler for Application-Specific Processor Arrays \(Zugl. Doktorarbeit\)](#)
(Dissertation, 1993)
BibTeX: [Download](#)
- Teich J., Thiele L.:
[Partitioning of processor arrays: A piecewise regular approach](#)

In: **Integration-The Vlsi Journal** (1993), p. 14(3):297-332

ISSN: 0167-9260

DOI: [10.1016/0167-9260\(93\)90013-3](https://doi.org/10.1016/0167-9260(93)90013-3)

BibTeX: [Download](#)

- Teich J., Thiele L., Zhang L.:

[Minimal communication in massively parallel architectures](#)

PARS Workshop 93 (Dresden, Germany,)

In: **Proc. of PARS Workshop 93** 1993

BibTeX: [Download](#)

1992

- Arzt U., Teich J., Schumacher M., Thiele L.:

[Hierarchical concepts in the design of processor arrays](#)

CompEuro 1992, (The Hague, The Netherlands,, 4. Mai 1992 - 8. Mai 1992)

In: **Proc. CompEuro 1992** 1992

DOI: [10.1109/CMPEUR.1992.218504](https://doi.org/10.1109/CMPEUR.1992.218504)

BibTeX: [Download](#)

- Arzt U., Teich J., Thiele L.:

[The concepts of COMPAR: A compiler for massive parallel architectures](#)

International Symposium on Circuits and Systems (ISCAS'92), (San Diego, CA, U.S.A.,)

In: **Proc. International Symposium on Circuits and Systems** 1992

BibTeX: [Download](#)

- Teich J., Thiele L.:

[A transformative approach to the partitioning of processor arrays](#)

Int. Conf. on Application Specific Array Processors (ASAP'92), (Berkeley, CA, U.S.A.,)

In: **Proc. Int. Conf. on Application Specific Array Processors** 1992

BibTeX: [Download](#)

- Teich J., Thiele L.:

[Control generation in the design of processor array](#)

In: **Parallel Processing on VLSI Arrays**, Kluwer Academic Publishers, 1992

BibTeX: [Download](#)

1991

- Teich J., Thiele L.:
[Control generation in the design of processor arrays](#)
In: **Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology** 3 (1991), p. 77-92
ISSN: 1387-5485
DOI: [10.1007/BF00927836](https://doi.org/10.1007/BF00927836)
BibTeX: [Download](#)
- Teich J., Thiele L.:
[Uniform design of parallel programs for DSP](#)
IEEE Int. Symp. Circuits and Systems (ISCAS) (Singapore)
In: **In Proc. IEEE Int. Symp. Circuits and Systems (ISCAS) 1991**
BibTeX: [Download](#)

1990

- Huber M., Teich J., Thiele L.:
[Design of configurable processor arrays](#)
IEEE Int. Symp. Circuits and Systems
In: **Proc. IEEE Int. Symp. Circuits and Systems 1990**
BibTeX: [Download](#)
- Teich J., Thiele L.:
[Systematic design concepts for signal processing arrays \(invited paper\)](#)
In: **Frequenz** 44 (1990), p. 122-132
ISSN: 0016-1136
DOI: [10.1515/FREQ.1990.44.3-4.122](https://doi.org/10.1515/FREQ.1990.44.3-4.122)
BibTeX: [Download](#)